

DOCUMENTATION TECHNIQUE

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GPS/Traceur SIMRAD CP33 pour navigation maritime

Caractéristiques



Généralités

Tension

d'alimentation: 12 et 24 V CC (10 à 32 V CC max) 8 à 17 watt

Câble

d'alimentation: Câble alimentation/NMEA, 2 m (Réf. 153-6070-002)

Dimensions: H:144 mm (5.8") L:252 mm (10") P:70 mm (2.8")

Poids: 1,5 kg (3.3 lbs)

Environnement: -10 à +55°C, IEC 60945, étanche selon les normes USC 46 CFR et IP55

Boîtier: Arrière en aluminium moulé, face avant en polycarbonate

Ecran: TFT couleur rétroéclairé: 5.7" 320 x 240 pixels, ou.....
STN monochrome translectif 6" 320 x 240 pixels

Présentation: 4 pages. Manuel, commutateur externe dédié, et séquençement automatique.

Interface: 1 port entrée/sortie NMEA 0183

1 port SimNet / NMEA 2000

Transfert PC: WPL et RTE

Alarme - sortie signal 5 V, 50 mA

Fusible: T6.3A temporisé (5x20 mm)

Réseau SimNet

Nombre maximum de produits connectés sur le réseau: 50

Longueur maximum du câblage (sans les 30m du capteur vent): 120 m (400')

Vitesse bus: 250 kbit/seconde

Courant maximum dans une prise SimNet:5A

Alimentation SimNet:..... 10.8 - 15 VDC

Longueur maximum d'un câble dérivé:.....6 m (20')

Longueur maximum de tous les câbles dérivés:60 m (200')

Étanchéité câblage: IP66

Température: max. 70°C (158°F)

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Section GPS

Récepteur: 14 canaux parallèles, code C/A, Filtre de Kalman 8 étages

Précision: Position (DGPS): 2 à 5 m RMS
Position (SDGPS): 3 à 7 m RMS
Position (GPS): 8 m RMS
Vitesse: 0.1 nœud
Cap: 1°

Filtre vitesse: 10 niveaux

Taux de mise

à jour: Intervalle 1 seconde, typique

Résistance

dynamique: Vitesse: 600 km/h
Accélération: 10 m / s²

	Antenne GPS RS5640	Antenne DGPS MGL-3
Type:	Quadrifilaire Helix	Patch et H-field
Dimensions:	L:230 mm Ø:38 mm	H:75 mm P:127 mm
Poids:	150 g (0.33 lbs)	600 g (1.3 lbs)

Environnement: -35°C à +75°C, humidité relative: 95%

Fixation: sur filetage 1" 14 (standard US)

Câble: RG58 10 m (standard), RG223 15 m (option), max. 30 m RG213

Section traceur

Système carto-

graphique: C-MAP NT+

Présentation: Carte semi dual - deux cartes à échelle et niveaux de détails spécifiques

Mémoire interne: Enregistrement dynamique avec capacité de combinaison jusqu'à
35,000 marques ou waypoints
10,000 waypoints avec nom (25 caractères)
50,000 points de tracés
50,000 sections de lignes
1,000 routes

Silicon Bipolar MMIC 5 GHz Active Double Balanced Mixer/IF Amp

Technical Data

IAM-81008

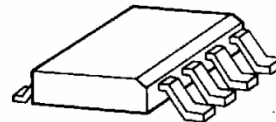
Features

- **RF-IF Conversion Gain From 0.05–5 GHz**
- **IF Conversion Gain From DC to 1 GHz**
- **Low Power Dissipation:**
65 mW at $V_{CC} = 5$ V Typical
- **Single Polarity Bias Supply:**
 $V_{CC} = 4$ to 8 V
- **Load-insensitive Performance**
- **Conversion Gain Flat Over Temperature**
- **Low LO Power Requirements:**
–5 dBm Typical
- **Low Cost Plastic Surface Mount Package**

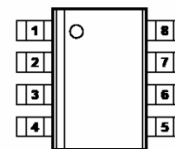
Typical applications include frequency down conversion, modulation, demodulation and phase detection. Markets include fiber-optics, GPS satellite navigation, mobile radio, and battery powered communications receivers.

The IAM series of Gilbert multiplier-based frequency converters is fabricated using HP's 10 GHz, f_T , 25 GHz f_{MAX} ISOSAT™-I silicon bipolar process. This process uses nitride self alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Plastic SO-8 Package



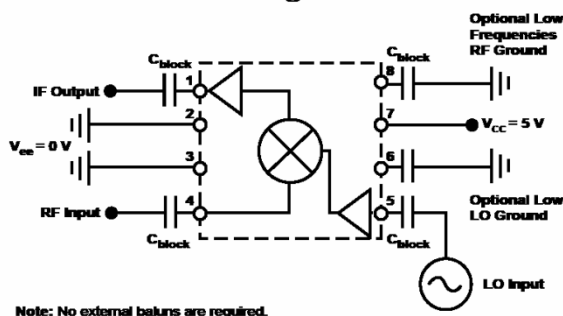
Pin Configuration



Description

The IAM-81008 is a complete low power consumption, double balanced active mixer housed in a miniature low cost plastic surface mount package. It is designed for narrow or wide bandwidth commercial and industrial applications having RF inputs up to 5 GHz. Operation at RF and LO frequencies less than 50 MHz can be achieved using optional external capacitors to ground. The IAM-81008 is particularly well suited for applications that require load-insensitive conversion and good spurious signal suppression with minimum LO and bias power consumption.

Typical Biasing Configuration and Functional Block Diagram



IAM-81008 Absolute Maximum Ratings

Parameter	Absolute Maximum ^[1]
Device Voltage	10 V
Power Dissipation ^{2,3}	300 mW
RF Input Power	+14 dBm
LO Input Power	+14 dBm
Junction Temperature	150°C
Storage Temperature	-65 to 150°C

Thermal Resistance:

$$\theta_{jc} = 80^{\circ}\text{C/W}$$

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{\text{CASE}} = 25^{\circ}\text{C}$.
3. Derate at 4.4 mW/°C for $T_{\text{C}} > 82^{\circ}\text{C}$.

IAM-81008 Part Number Ordering Information

Part Number	Devices Per Reel	Reel Size
IAM-81008-TR1	1000	7"

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

IAM-81008 Electrical Specifications^[1], $T_A = 25^{\circ}\text{C}$

Symbol	Parameters and Test Conditions: $V_{cc} = 5\text{ V}$, $Z_0 = 50\ \Omega$, LO = -5 dBm, RF = -20 dBm	Units	Min.	Typ.	Max.
G_C	Conversion Gain RF = 2 GHz, LO = 1.75 GHz	dB	6.0	8.5	10
$F_{3\text{ dB RF}}$	RF Bandwidth (G_C 3 dB Down) IF = 250 MHz	GHz		3.5	
$F_{3\text{ dB IF}}$	IF Bandwidth (G_C 3 dB Down) LO = 2 GHz	GHz		0.6	
$P_{1\text{ dB}}$	IF Output Power at 1 dB Gain Compression RF = 2 GHz, LO = 1.75 GHz	dBm		-6	
IP_3	IF Output Third Order Intercept Point RF = 2 GHz, LO = 1.75 GHz	dBm		3	
NF	SSB Noise Figure RF = 2 GHz, LO = 1.75 GHz	dB		17	
VSWR	RF Port VSWR $f = 0.05$ to 3.5 GHz			1.5:1	
	LO Port VSWR $f = 0.05$ to 3.5 GHz			2.0:1	
	IF Port VSWR $f < 1$ GHz			1.5:1	
RF_{if}	RF Feedthrough at IF Port RF = 2 GHz, LO = 1.75 GHz	dBc		-25	
LO_{if}	LO Leakage at IF Port LO = 1.75 GHz	dBm		-25	
LO_{rf}	LO Leakage at RF Port LO = 1.75 GHz	dBm		-30	
I_{CC}	Supply Current	mA	10	13	16

Note:

1. The recommended operating voltage range for this device is 4 to 8 V. Typical performance as a function of voltage is on the following page.

High performance low power mixer FM IF system

NE/SA615

DESCRIPTION

The NE/SA615 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA615 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC} , lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters

PIN CONFIGURATION

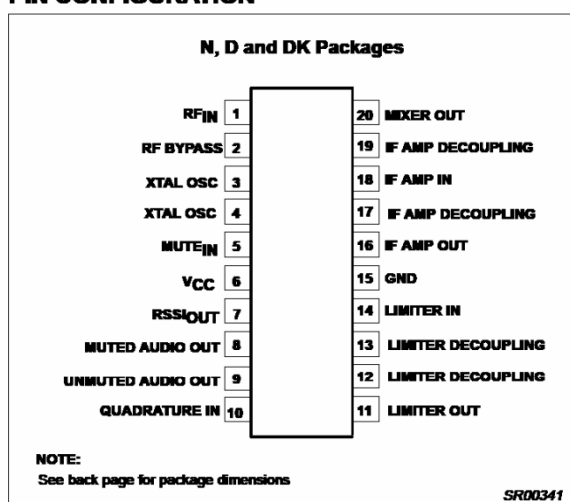


Figure 1. Pin Configuration

- Excellent sensitivity: 0.22 μ V into 50 Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA615 meets cellular radio specifications
- ESD hardened

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE615N	SOT146-1
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA615N	SOT146-1
20-Pin Plastic Small Outline Large (SOL) package	0 to +70°C	NE615D	SOT108-1
20-Pin Plastic Small Outline Large (SOL) package	-40 to +85°C	SA615D	SOT108-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE615DK	SOT266-1
20-Pin Plastic Shrink Small Outline Package (SSOP)	-40 to +85°C	SA615DK	SOT266-1

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High performance low power mixer FM IF system

NE/SA615

BLOCK DIAGRAM

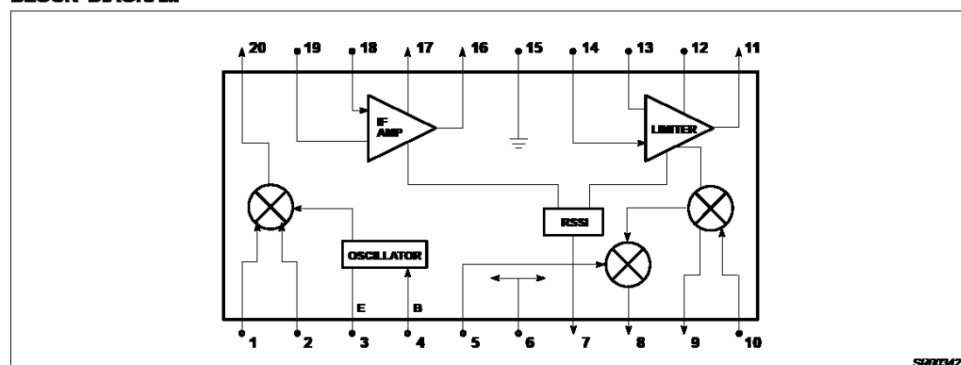


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE615	0 to +70	°C
	SA615	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	
	SSOP package	117	

DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = +6V$, $T_A = 25^\circ C$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
V _{CC}	Power supply voltage range		4.5		8.0	V
I _{CC}	DC current drain			5.7	7.4	mA
	Mute switch input threshold (ON)		1.7			V
	(OFF)				1.0	V

CIRCUIT DESCRIPTION

The NE/SA615 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source.

However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

High performance low power mixer FM IF system

NE/SA615

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$; $V_{CC} = +6\text{V}$, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; $R_{17} = 5.1\text{k}$; RF level = -45dBm; FM modulation = 1kHz with $\pm 8\text{kHz}$ peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 3. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)						
f _{IN}	Input signal frequency			500		MHz
f _{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up 50Ω source	8.0	13		dB
				-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R ₁₇ = 5.1k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, R ₁₀ = 100k	15nF de-emphasis	60	150	260	mV _{RM S}
	Unmuted audio level, R ₁₁ = 100k	150pF de-emphasis		530		mV
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, R ₉ = 100kΩ ¹	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	R ₉ = 100kΩ Pin 16		80		dB
	RSSI accuracy	R ₉ = 100kΩ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (int LO)						
	Unmuted audio level	4.5V = V _{CC} , RF level = -27dBm		450		mV _{RM S}
	System RSSI output	4.5V = V _{CC} , RF level = -27dBm		4.3		V

NOTE:

1. The generator source impedance is 50 Ω , but the NE/SA605 input impedance at Pin 18 is 1500 Ω . As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

BIPOLAR DIGITAL INTEGRATED CIRCUITS

μ PB1506GV, μ PB1507GV

3GHz INPUT DIVIDE BY 256, 128, 64 PRESCALER IC FOR ANALOG DBS TUNERS

The μ PB1506GV and μ PB1507GV are 3.0 GHz input, high division silicon prescaler ICs for analog DBS tuner applications. These ICs divide-by-256, 128 and 64 contribute to produce analog DBS tuners with kit-use of 17 K series DTS controller or standard CMOS PLL synthesizer IC. The μ PB1506GV/ μ PB1507GV are shrink package versions of the μ PB586G/588G or μ PB1505GR so that these smaller packages contribute to reduce the mounting space replacing from conventional ICs.

The μ PB1506GV and μ PB1507GV are manufactured using NEC's high fr NESAT™IV silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, these ICs have excellent performance, uniformity and reliability.

FEATURES

- High toggle frequency : f_{in} = 0.5 GHz to 3.0 GHz
- High-density surface mounting : 8-pin plastic SSOP (175 mil)
- Low current consumption : 5 V, 19 mA
- Selectable high division : $\div 256$, $\div 128$, $\div 64$
- Pin connection variation : μ PB1506GV and μ PB1507GV

APPLICATION

These ICs can use as a prescaler between local oscillator and PLL frequency synthesizer included modulus prescaler. For example, following application can be chosen;

- Analog DBS tuner's synthesizer
- Analog CATV converter synthesizer

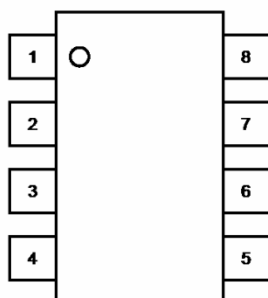
ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING	SUPPLYING FORM
μ PB1506GV-E1	8-pin plastic	1506	Embossed tape 8 mm wide. Pin 1 is in tape pull-out direction. 1 000 p/reel.
μ PB1507GV-E1	SSOP (175 mil)	1507	

Remarks To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μ PB1506GV, μ PB1507GV)

Caution: Electro-static sensitive devices

PIN CONNECTION (Top View)



Pin NO.	μPB1506GV	μPB1507GV
1	SW1	IN
2	IN	V _{CC}
3	IN	SW1
4	GND	OUT
5	NC	GND
6	SW2	SW2
7	OUT	NC
8	V _{CC}	IN

PIN EXPLANATION

Pin name	Applied voltage V	Pin voltage V	Functions and explanation	Pin no.														
				μPB1506GV	μPB1507GV													
IN	—	2.9	Signal input pin. This pin should be coupled to signal source with capacitor (e.g. 1 000 pF) for DC cut.	2	1													
IN	—	2.9	Signal input bypass pin. This pin must be equipped with bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.	3	8													
GND	0	—	Ground pin. Ground pattern on the board should be formed as wide as possible to minimize ground impedance.	4	5													
SW1	H/L	—	Divide ratio input pin. The ratio can be determined by following applied level to these pins. <div><table><tr><td colspan="2" rowspan="2"></td><th colspan="2">SW2</th></tr><tr><th>H</th><th>L</th></tr><tr><th rowspan="2">SW1</th><th>H</th><td>±64</td><td>±128</td></tr><tr><th>L</th><td>±128</td><td>±256</td></tr></table></div>			SW2		H	L	SW1	H	±64	±128	L	±128	±256	1	3
		SW2																
		H	L															
SW1	H	±64	±128															
	L	±128	±256															
SW2			These pins should be equipped with bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.	6	6													
Vcc	4.5 to 5.5	—	Power supply pin. This pin must be equipped with bypass capacitor (e.g. 10 000 pF) to minimize ground impedance.	8	2													
OUT	—	2.6 to 4.7	Divided frequency output pin. This pin is designed as emitter follower output. This pin can be connected to CMOS input due to 1.2 V _{P-P} MIN output.	7	4													
NC	—	—	Non connection pin. This pin must be opened.	5	7													



UPC2709T, UPC2712T

2.5 GHz SILICON MMIC WIDE-BAND AMPLIFIER

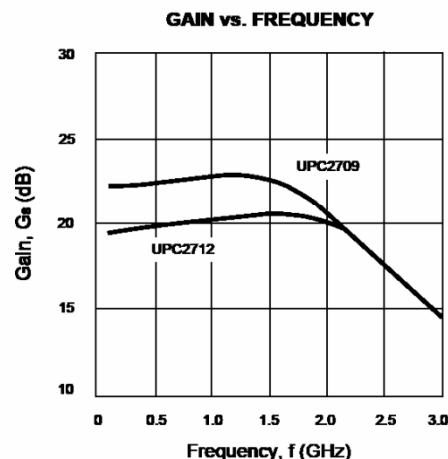
FEATURES

- **WIDE FREQUENCY RESPONSE:** 2.5 GHz
- **HIGH GAIN:** 23 dB (UPC2709T)
- **SATURATED OUTPUT POWER:** +11.5 dBm (UPC2709T)
- **INTERNAL CURRENT REGULATION MINIMIZES GAIN CHANGE OVER TEMPERATURE**
- **5 V SINGLE SUPPLY VOLTAGE**
- **SUPER SMALL PACKAGE**
- **TAPE AND REEL PACKAGING OPTION AVAILABLE**

DESCRIPTION

NEC's UPC2709T and UPC2712T are Silicon Monolithic integrated circuits manufactured using the NESAT III process. These devices are suitable as buffer amplifiers for wide-band applications. They are designed for low cost gain stages in cellular radios, GPS receivers, DBS tuners, PCN, and test/measurement equipment.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.



ELECTRICAL CHARACTERISTICS (TA = 25°C, f = 1 GHz, Vcc = 5 V)

PART NUMBER PACKAGE OUTLINE			UPC2709T T06			UPC2712T T06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX
Icc	Circuit Current (no signal)	mA	19	25	32	9	12	15
Gs	Small Signal Gain	dB	21	23	26.5	18	20	23.5
fu	Upper Limit Operating Frequency (The gain at fu is 3 dB down from the gain at 0.1 GHz)	GHz	2.0	2.3		2.2	2.6	
ΔGs	Gain Flatness, f = 0.1 ~ 1.8 GHz f = 0.1 ~ 2.0 GHz	dB		±1.0			±0.8	
Psat	Saturated Output Power	dBm	9	11.5		0	3	
P1dB	Output Power at 1 dB Compression Point	dBm		7.5			-2.5	
NF	Noise Figure	dB		5	6.5		4.5	6
RLin	Input Return Loss	dB	7	10		9	12	
RLout	Output Return Loss	dB	7	10		10	13	
ISOL	Isolation	dB	26	31		28	33	
ΔGT	Gain -Temperature Coefficient	dB/°C		-0.002			-0.003	
Rth	Thermal Resistance (Junction to Ambient)	°C/W			200			200

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Date Published: June 28, 2005

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NEC

1.9 GHz BANDWIDTH GENERAL PURPOSE SILICON MMIC AMPLIFIER

UPC1675G

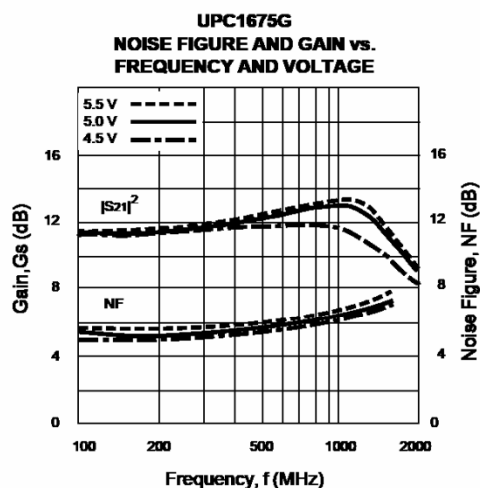
FEATURES

- **WIDE BANDWIDTH:**
1900 MHz at 3 dB Point
- **HIGH ISOLATION**
- **SINGLE POWER SUPPLY:** $V_{CC} = 5\text{ V}$
- **INPUT/OUTPUT MATCHED TO $50\ \Omega$**
- **AVAILABLE IN TAPE AND REEL**

DESCRIPTION

The UPC1675G is a silicon monolithic integrated circuit designed for wide-band amplifiers covering the HF to UHF bands. This device is available in a surface mount package.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $f = 500\text{ MHz}$)

PART NUMBER PACKAGE OUTLINE			UPC1675G 39		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I_{CC}	Supply Current	mA	12	17	22
G_s	Small Signal Gain	dB	10	12	14
$PSAT$	Saturated Output Power	dBm	2	4	
BW^1	Bandwidth	MHz	1600	1900	
NF	Noise Figure	dB		5.5	7
RL_{IN}	Input Return Loss	dB	9	12	
RL_{OUT}	Output Return Loss	dB	8	11	
ISOL	Isolation	dB	21	24.5	

Note:

1. Gain is 3 dB down from gain at 100 MHz.

California Eastern Laboratories

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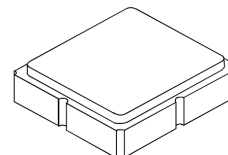


- RF Filter for GPS Receiver
- Surface-mount 3.0 x 3.0 mm Package
- Complies with Directive 2002/95/EC (RoHS)



SF1186B-4

**1575 MHz
SAW Filter**



SM3030-8

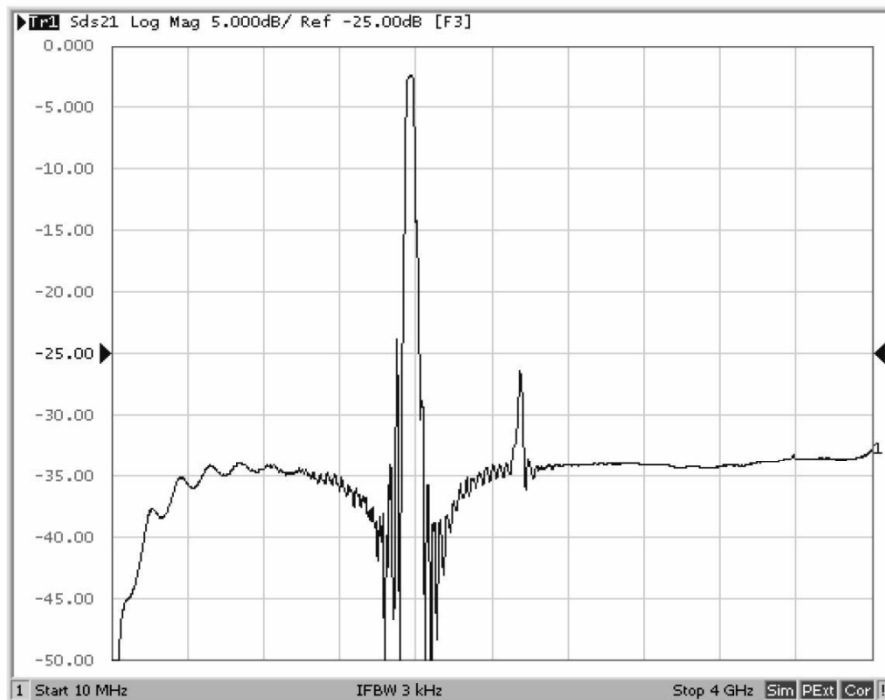
Absolute Maximum Ratings

Rating	Value	Units
Input Power Level	10	dBm
DC Voltage on any Non-ground Terminal	3	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range in Tape and Reel	-40 to +85	°C
Maximum Soldering Profile, 5 cycles/ 10 seconds maximum	265	°C

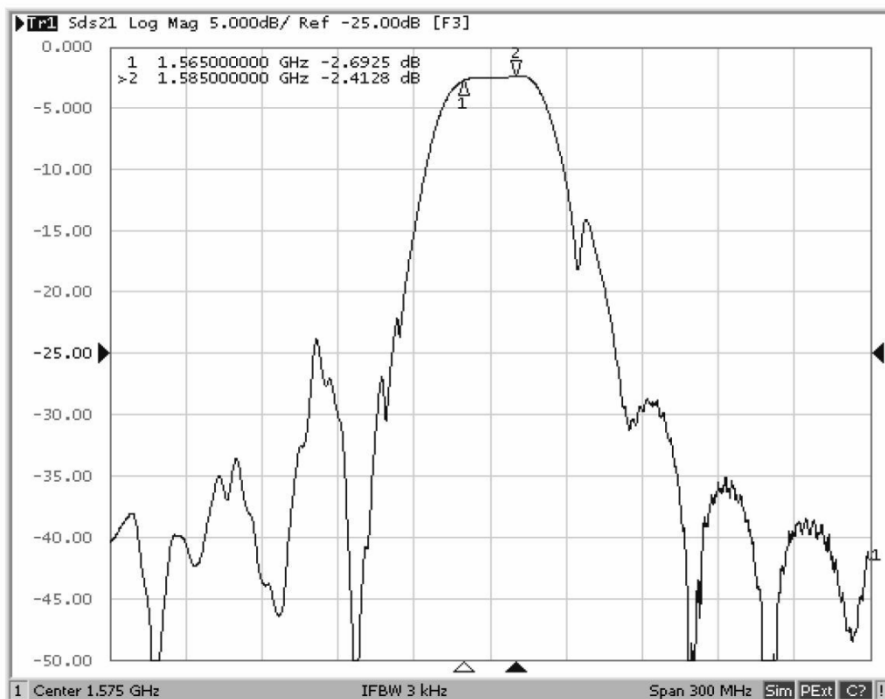
Electrical Characteristics

Characteristic	Sym	Notes	Min	Typ	Max	Units
Center Frequency	f _C			1575		MHz
Insertion Loss, 1565 - 1585 MHz	IL			2.7	4.5	dB
Amplitude Ripple, 1565 - 1585 MHz				0.4	1.5	dB
Attenuation, 0 dB Reference:						dB
0 to 1000 MHz			32	34		
1000 to 1435 MHz			32	34.5		
1435 to 1525 MHz			22	24		
1525 to 1540 MHz			7	21		
1610 to 1625 MHz			7	16		
1625 to 1715 MHz			22	25.5		
1715 to 1785 MHz			34	39		
1785 to 2100 MHz			30	34		
2100 to 2200 MHz			25	26.5		
2200 to 2500 MHz			27	34		
2500 to 4000 MHz			18	32		
Source Impedance, Unbalanced	Z _S			50		Ω
Load Impedance, Balanced	Z _L			50		
Case Style	SM3030-8 3.0 x 3.0 mm Nominal Footprint					
Lid Symbolization (Y=year, WW=week, S=shift) dot=pin 1 indicator	905, YWWS					
Standard Reel Quantity	Reel Size 7 Inch	500 Pieces/Reel				
	Reel Size 13 Inch	3000 Pieces/Reel				

Filter Wideband Response



Filter Passband Response



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High speed CAN transceiver

TJA1050

FEATURES

- Fully compatible with the "ISO 11898" standard
- High speed (up to 1 Mbaud)
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with wide common-mode range for high ElectroMagnetic Immunity (EMI)
- An unpowered node does not disturb the bus lines
- Transmit Data (TXD) dominant time-out function
- Silent mode in which the transmitter is disabled
- Bus pins protected against transients in an automotive environment
- Input levels compatible with 3.3 V and 5 V devices
- Thermally protected
- Short-circuit proof to battery and to ground
- At least 110 nodes can be connected.

GENERAL DESCRIPTION

The TJA1050 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The TJA1050 is the third Philips high-speed CAN transceiver after the PCA82C250 and the PCA82C251. The most important differences are:

- Much lower electromagnetic emission due to optimal matching of the output signals CANH and CANL
- Improved behaviour in case of an unpowered node
- No standby mode.

This makes the TJA1050 eminently suitable for use in nodes that are in a power-down situation in partially powered networks.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.25	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	-27	+40	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	-27	+40	V
$V_{i(dif)(bus)}$	differential bus input voltage	dominant	1.5	3	V
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	$V_S = 0$ V; see Fig.7	–	250	ns
T_{vj}	virtual junction temperature		-40	+150	°C

PINNING

SYMBOL	PIN	DESCRIPTION
TXD	1	transmit data input; reads in data from the CAN controller to the bus line drivers
GND	2	ground
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines to the CAN controller
V_{ref}	5	reference voltage output
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
S	8	select input for high-speed mode or silent mode

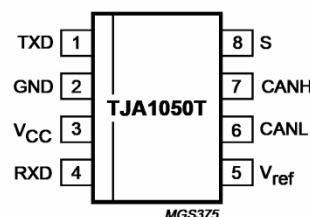


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TJA1050 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for high-speed automotive applications using baud rates from 60 kbaud up to 1 Mbaud. It provides differential transmit capability to the bus and differential receiver capability to the CAN protocol controller. It is fully compatible to the "ISO 11898" standard.

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 165 °C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when pin TXD goes HIGH. The thermal protection circuit is particularly needed when a bus line short-circuits.

The pins CANH and CANL are protected from automotive electrical transients (according to "ISO 7637", see Fig.4).

Control pin S allows two operating modes to be selected: high-speed mode or silent mode.

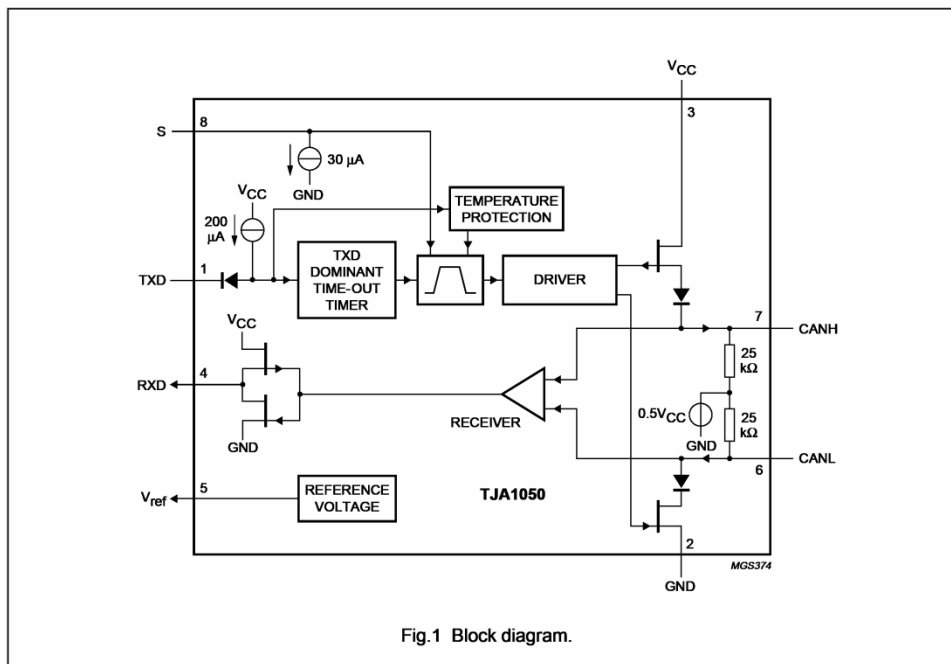
The high-speed mode is the normal operating mode and is selected by connecting pin S to ground. It is the default mode if pin S is not connected. However, to ensure EMI performance in applications using only the high-speed mode, it is recommended that pin S is connected to ground.

In the silent mode, the transmitter is disabled. All other IC functions continue to operate. The silent mode is selected by connecting pin S to V_{CC} and can be used to prevent network communication from being blocked, due to a CAN controller which is out of control.

A 'TXD dominant time-out' timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW-level on pin TXD exceeds the internal timer value, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TXD.

Table 1 Function table of the CAN transceiver; X = don't care

V_{CC}	TXD	S	CANH	CANL	BUS STATE	RXD
4.75 V to 5.25 V	LOW	LOW (or floating)	HIGH	LOW	dominant	LOW
4.75 V to 5.25 V	X	HIGH	$0.5V_{CC}$	$0.5V_{CC}$	recessive	HIGH
4.75 V to 5.25 V	HIGH (or floating)	X	$0.5V_{CC}$	$0.5V_{CC}$	recessive	HIGH
<2 V (not powered)	X	X	$0 V < V_{CANH} < V_{CC}$	$0 V < V_{CANL} < V_{CC}$	recessive	X
$2 V < V_{CC} < 4.75 V$	>2 V	X	$0 V < V_{CANH} < V_{CC}$	$0 V < V_{CANL} < V_{CC}$	recessive	X

BLOCK DIAGRAM

High speed CAN transceiver

TJA1050

CHARACTERISTICS

$V_{CC} = 4.75\text{ V}$ to 5.25 V ; $T_{vj} = -40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$; $R_L = 60\text{ }\Omega$ unless specified otherwise; all voltages are referenced to GND (pin 2); positive currents flow into the IC; see notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin V _{CC})						
I _{CC}	supply current	dominant; V _{TXD} = 0 V	25	50	75	mA
		recessive; V _{TXD} = V _{CC}	2.5	5	10	mA
Transmitter data input (pin TXD)						
V _{IH}	HIGH-level input voltage	output recessive	2.0	–	V _{CC} + 0.3	V
V _{IL}	LOW-level input voltage	output dominant	–0.3	–	+0.8	V
I _{IH}	HIGH-level input current	V _{TXD} = V _{CC}	–5	0	+5	μA
I _{IL}	LOW-level input current	V _{TXD} = 0 V	–100	–200	–300	μA
C _i	input capacitance	not tested	–	5	10	pF
Mode select input (pin S)						
V _{IH}	HIGH-level input voltage	silent mode	2.0	–	V _{CC} + 0.3	V
V _{IL}	LOW-level input voltage	high-speed mode	–0.3	–	+0.8	V
I _{IH}	HIGH-level input current	V _S = 2 V	20	30	50	μA
I _{IL}	LOW-level input current	V _S = 0.8 V	15	30	45	μA
Receiver data output (pin RXD)						
I _{OH}	HIGH-level output current	V _{RXD} = 0.7V _{CC}	–2	–6	–15	mA
I _{OL}	LOW-level output current	V _{RXD} = 0.45 V	2	8.5	20	mA
Reference voltage output (pin V _{ref})						
V _{ref}	reference output voltage	–50 μA < I _{Vref} < +50 μA	0.45V _{CC}	0.5V _{CC}	0.55V _{CC}	V
Bus lines (pins CANH and CANL)						
V _{o(reces)} (CANH)	recessive bus voltage at pin CANH	V _{TXD} = V _{CC} ; no load	2.0	2.5	3.0	V
V _{o(reces)} (CANL)	recessive bus voltage at pin CANL	V _{TXD} = V _{CC} ; no load	2.0	2.5	3.0	V
I _{o(reces)} (CANH)	recessive output current at pin CANH	–27 V < V _{CANH} < +32 V; 0 V < V _{CC} < 5.25 V	–2.0	–	+2.5	mA
I _{o(reces)} (CANL)	recessive output current at pin CANL	–27 V < V _{CANL} < +32 V; 0 V < V _{CC} < 5.25 V	–2.0	–	+2.5	mA
V _{o(dom)} (CANH)	dominant output voltage at pin CANH	V _{TXD} = 0 V	3.0	3.6	4.25	V
V _{o(dom)} (CANL)	dominant output voltage at pin CANL	V _{TXD} = 0 V	0.5	1.4	1.75	V
V _{i(dif)} (bus)	differential bus input voltage (V _{CANH} – V _{CANL})	V _{TXD} = 0 V; dominant; 42.5 Ω < R _L < 60 Ω	1.5	2.25	3.0	V
		V _{TXD} = V _{CC} ; recessive; no load	–50	0	+50	mV

HCPL0600, HCPL0601, HCPL0611, HCPL0637, HCPL0638, HCPL0639 High Speed-10 MBit/s Logic Gate Optocouplers

Single Channel: HCPL0600, HCPL0601, HCPL0611
Dual Channel: HCPL0637, HCPL0638, HCPL0639

Features

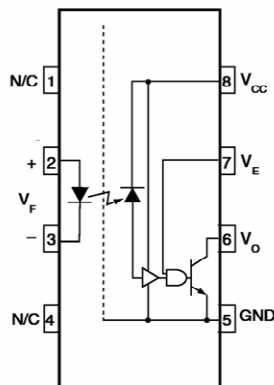
- Compact SO8 package
- Very high speed-10 MBit/s
- Superior CMR
- Logic gate output
- Storable output (single channel devices)
- Wired OR-open collector
- U.L. recognized (File # E90700)
- IEC60747-5-2 approved (VDE option)
 - HCPL0600, HCPL0601, HCPL0611 only

Applications

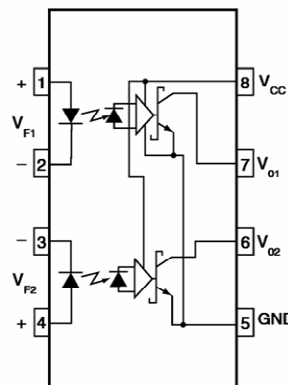
- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

Description

The HCPL06XX optocouplers consist of an AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a storable output (single channel devices). The devices are housed in a compact small-outline package. This output features an open collector, thereby permitting wired OR outputs. The HCPL0600, HCPL0601 and HCPL0611 output consists of bipolar transistors on a bipolar process while the HCPL0637, HCPL0638, and HCPL0639 output consists of bipolar transistors on a CMOS process for reduced power consumption. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. An internal noise shield provides superior common mode rejection.



Single-channel circuit drawing
(HCPL0600, HCPL0601 and HCPL0611)



Dual-channel circuit drawing
(HCPL0637, HCPL0638 and HCPL0639)

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H*	NC*	L*
L*	NC*	H*

*Dual channel devices or single channel devices with pin 7 not connected.
 A 0.1µF bypass capacitor must be connected between pins 8 and 5. (See note 1)

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Electrical Characteristics ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise specified.)
Individual Component Characteristics

Symbol	Parameter	Test Conditions			Min.	Typ.*	Max.	Unit
EMITTER								
V _F	Input Forward Voltage	I _F = 10mA					1.8	V
			T _A = 25°C				1.75	
B _{VR}	Input Reverse Breakdown Voltage	I _R = 10μA			5.0			V
ΔV _F /ΔT _A	Input Diode Temperature Coefficient	I _F = 10mA				-1.5		mV/°C
DETECTOR								
I _{CCH}	High Level Supply Current	I _F = 0mA, V _{CC} = 5.5V	V _E = 0.5 V	Single Channel			10	mA
				Dual Channel			15	
I _{CCL}	Low Level Supply Current	I _F = 10mA, V _{CC} = 5.5V	V _E = 0.5 V	Single Channel			13	mA
				Dual Channel			21	
I _{EL}	Low Level Enable Current	V _{CC} = 5.5V, V _E = 0.5V		Single Channel			-1.6	mA
I _{EH}	High Level Enable Current	V _{CC} = 5.5V, V _E = 2.0V		Single Channel			-1.6	mA
V _{EH}	High Level Enable Voltage	V _{CC} = 5.5V, I _F = 10mA		Single Channel	2.0			V
V _{EL}	Low Level Enable Voltage	V _{CC} = 5.5V, I _F = 10mA ⁽²⁾		Single Channel			0.8	V

Typical Performance Curves (HCPL0600, HCPL0601 and HCPL0611 only)

Fig. 1 Forward Current vs. Input Forward Voltage

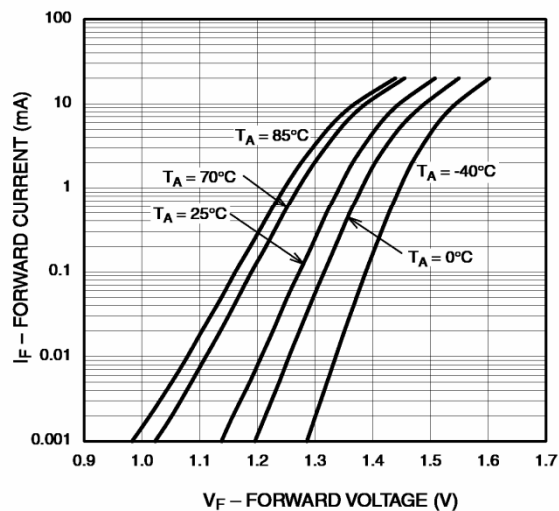


Fig. 2 Output Voltage vs. Forward Current

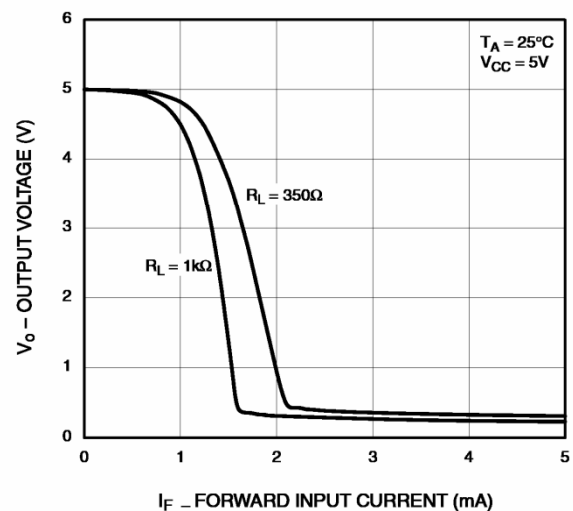
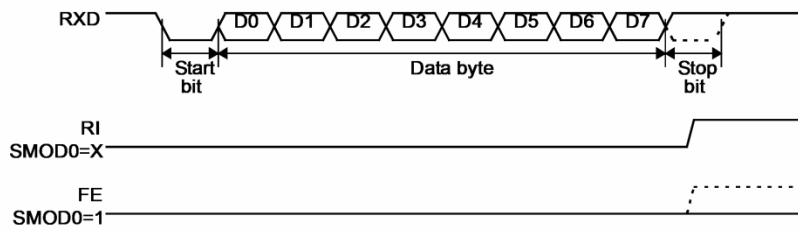


Figure 29. UART Timing in Mode 1



T89C51CC01 : UART

Figure 30. UART Timing in Modes 2 and 3

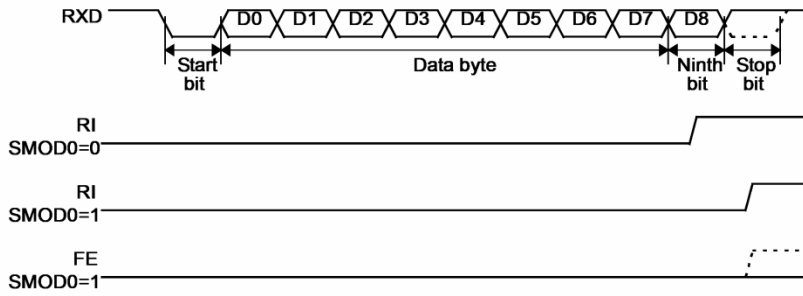


Table 34. PCON Register

PCON (S:87h)

Power Control Register

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	General-purpose Flag Cleared by user for general-purpose usage. Set by user for general-purpose usage.					
2	GF0	General-purpose Flag Cleared by user for general-purpose usage. Set by user for general-purpose usage.					
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Table 30. SCON Register

SCON (S:98h)

Serial Control Register

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Bit Number	Bit Mnemonic	Description					
7	FE	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected.					
	SM0	Serial port Mode bit 0 (SMOD0=0) Refer to SM1 for serial port mode selection.					
6	SM1	Serial port Mode bit 1 SM0SM1Mode Baud Rate 0 0 Shift Register $F_{XTAL}/12$ (or $F_{XTAL}/6$ in mode X2) 0 1 8-bit UARTVariable 1 0 9-bit UART $F_{XTAL}/64$ or $F_{XTAL}/32$ 1 1 9-bit UARTVariable					
5	SM2	Serial port Mode 2 bit/Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3.					
4	REN	Reception Enable bit Clear to disable serial reception. Set to enable serial reception.					
3	TB8	Transmitter Bit 8/Ninth bit to transmit in modes 2 and 3 Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.					
2	RB8	Receiver Bit 8/Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1.					
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.					
0	RI	Receive Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 29. and Figure 30. in the other modes.					

T89C51CC01 : TIMER1

Mode 2 (8-bit Timer with Auto-Reload)

Mode 2 configures Timer 1 as an 8-bit Timer (TL1 register) that automatically reloads from TH1 register (see Figure 33). TL1 overflow sets TF1 flag in TCON register and reloads TL1 with the contents of TH1, which is preset by software. When the interrupt request is serviced, hardware clears TF1. The reload leaves TH1 unchanged. The next reload value may be changed at any time by writing it to TH1 register.

Figure 33. Timer/Counter x (x = 0 or 1) in Mode 2

See the "Clock" section

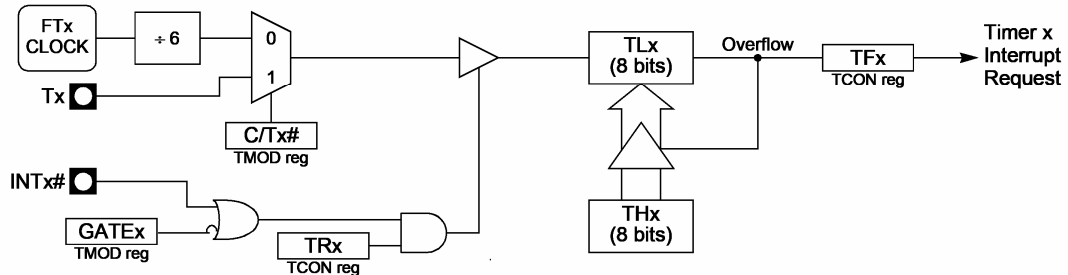


Table 36. TMOD Register

TMOD (S:89h)
Timer/Counter Mode Control Register

7	6	5	4	3	2	1	0
GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
Bit Number	Bit Mnemonic	Description					
7	GATE1	Timer 1 Gating Control Bit Clear to enable Timer 1 whenever TR1 bit is set. Set to enable Timer 1 only while INT1# pin is high and TR1 bit is set.					
6	C/T1#	Timer 1 Counter/Timer Select Bit Clear for Timer operation: Timer 1 counts the divided-down system clock. Set for Counter operation: Timer 1 counts negative transitions on external pin T1.					
5	M11	Timer 1 Mode Select Bits M11M01Operating mode					
4	M01	0 0Mode 0: 8-bit Timer/Counter (TH1) with 5-bit prescaler (TL1). 0 1Mode 1: 16-bit Timer/Counter. 1 0Mode 2: 8-bit auto-reload Timer/Counter (TL1) ⁽¹⁾ 1 1Mode 3: Timer 1 halted. Retains count					
3	GATE0	Timer 0 Gating Control Bit Clear to enable Timer 0 whenever TR0 bit is set. Set to enable Timer/Counter 0 only while INT0# pin is high and TR0 bit is set.					
2	C/T0#	Timer 0 Counter/Timer Select Bit Clear for Timer operation: Timer 0 counts the divided-down system clock. Set for Counter operation: Timer 0 counts negative transitions on external pin T0.					
1	M10	Timer 0 Mode Select Bit M10M00Operating mode					
0	M00	0 0Mode 0: 8-bit Timer/Counter (TH0) with 5-bit prescaler (TL0). 0 1Mode 1: 16-bit Timer/Counter. 1 0Mode 2: 8-bit auto-reload Timer/Counter (TL0) ⁽²⁾ 1 1Mode 3: TL0 is an 8-bit Timer/Counter TH0 is an 8-bit Timer using Timer 1's TR0 and TF0 bits.					

Table 35. TCON Register

TCON (S:88h)
Timer/Counter Control Register

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Bit Number	Bit Mnemonic	Description					
7	TF1	Timer 1 Overflow Flag Cleared by hardware when processor vectors to interrupt routine. Set by hardware on Timer/Counter overflow, when Timer 1 register overflows.					
6	TR1	Timer 1 Run Control Bit Clear to turn off Timer/Counter 1. Set to turn on Timer/Counter 1.					
5	TF0	Timer 0 Overflow Flag Cleared by hardware when processor vectors to interrupt routine. Set by hardware on Timer/Counter overflow, when Timer 0 register overflows.					
4	TR0	Timer 0 Run Control Bit Clear to turn off Timer/Counter 0. Set to turn on Timer/Counter 0.					
3	IE1	Interrupt 1 Edge Flag Cleared by hardware when interrupt is processed if edge-triggered (see IT1). Set by hardware when external interrupt is detected on INT1# pin.					
2	IT1	Interrupt 1 Type Control Bit Clear to select low level active (level triggered) for external interrupt 1 (INT1#). Set to select falling edge active (edge triggered) for external interrupt 1.					
1	IE0	Interrupt 0 Edge Flag Cleared by hardware when interrupt is processed if edge-triggered (see IT0). Set by hardware when external interrupt is detected on INT0# pin.					
0	IT0	Interrupt 0 Type Control Bit Clear to select low level active (level triggered) for external interrupt 0 (INT0#). Set to select falling edge active (edge triggered) for external interrupt 0.					

Table 39. TH1 Register

TH1 (S:8Dh)
Timer 1 High Byte Register

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–
Bit Number	Bit Mnemonic	Description					
7:0		High Byte of Timer 1.					

Table 40. TL1 Register

TL1 (S:8Bh)
Timer 1 Low Byte Register

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–
Bit Number	Bit Mnemonic	Description					
7:0		Low Byte of Timer 1.					