MONITEUR MULTIPARAMÈTRE COLIN BP306

DOSSIER TECHNIQUE

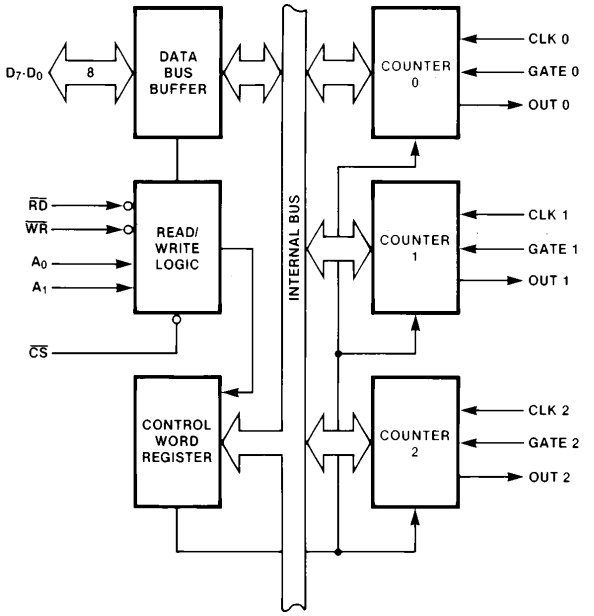
(21 pages)

8254
PROGRAMMABLE INTERVAL TIMER

- **Compatible with All Intel and Most Other Microprocessors**
- **Handles Inputs from DC to 10 MHz**
  — 8 MHz 8254
  — 10 MHz 8254-2
- **Status Read-Back Command**
- **Six Programmable Counter Modes**
- **Three Independent 16-Bit Counters**
- **Binary or BCD Counting**
- **Single +5V Supply**
- **Available in EXPRESS**
  — Standard Temperature Range

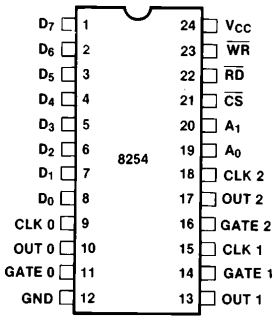
The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.



231164-1

Figure 1. 8254 Block Diagram



231164-2

Figure 2. Pin Configuration

September 1993

Order Number: 231164-005

Control Word Format

A_1,A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 7. Control Word Format

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1,A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Write Operations

The programming procedure for the 8254 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.
2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1,A_0 inputs), and each Control Word specifies the Counter it applies to (SC0,SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions in Figure 7 is acceptable.

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Mode Definitions

The following are defined for use in describing the operation of the 8254.

CLK Pulse: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

Trigger: a rising edge of a Counter's GATE input.

Counter loading: the transfer of a count from the CR to the CE (refer to the ''Functional Description'')

MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required)
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the

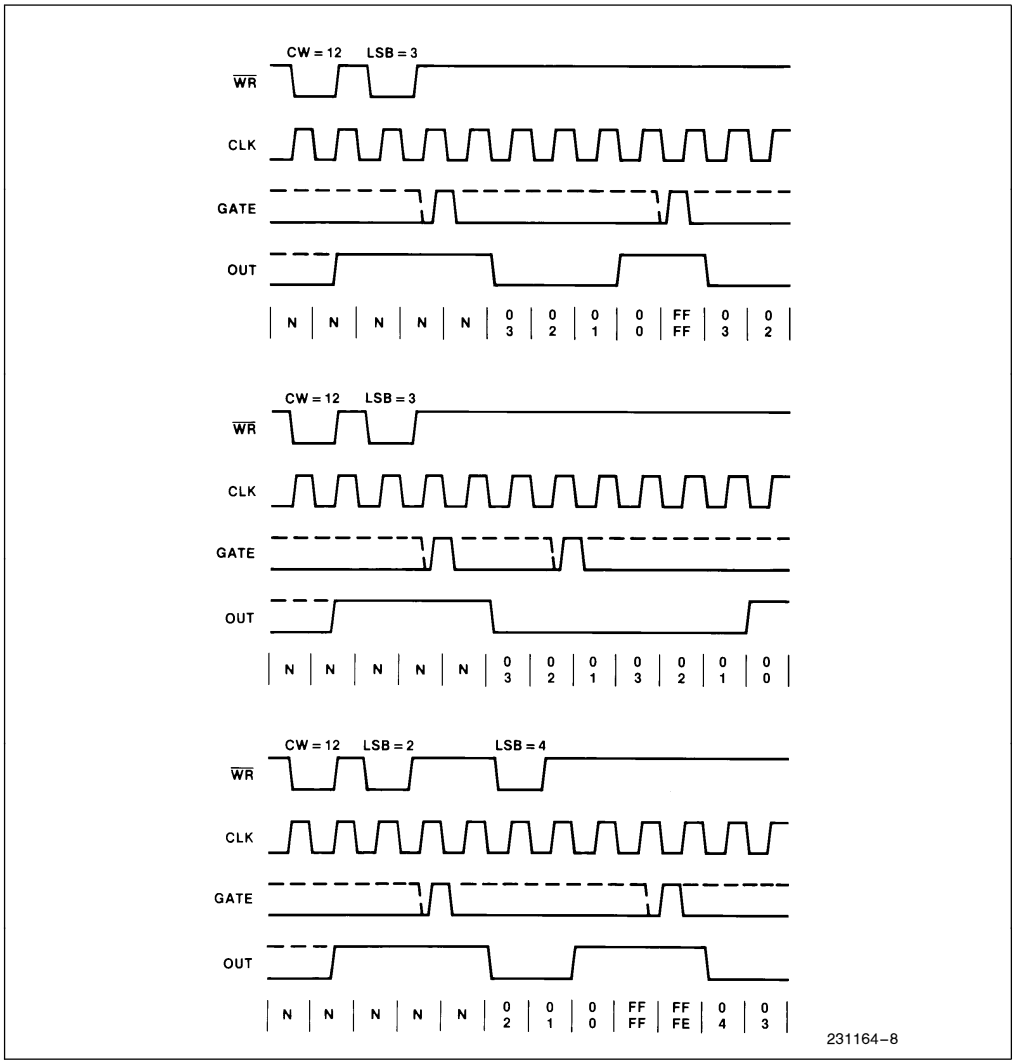


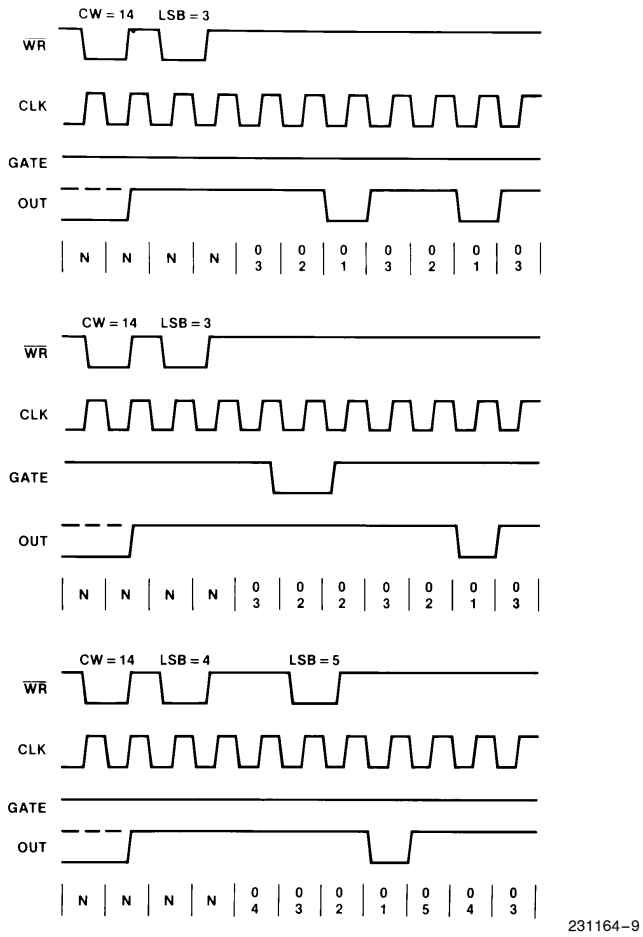
Figure 16. Mode 1

initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the



NOTE:
A GATE transition should not occur one clock prior to terminal count.

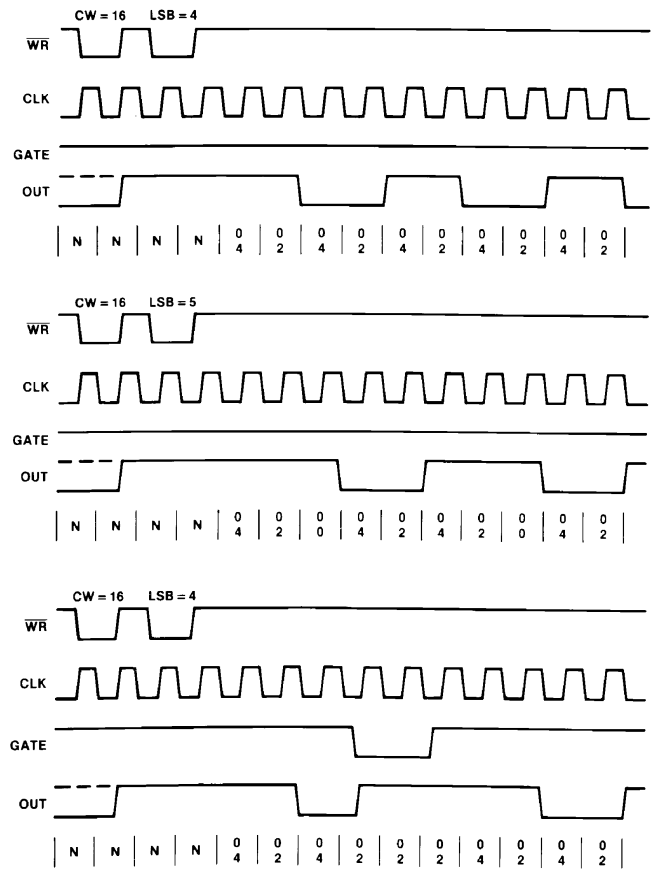
Figure 17. Mode 2

new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse *after* the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for $(N + 1)/2$ counts and low for $(N - 1)/2$ counts.



NOTE:
A GATE transition should not occur one clock prior to terminal count.

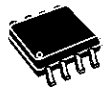
Figure 18. Mode 3

TL431

PROGRAMMABLE VOLTAGE REFERENCE

- ADJUSTABLE OUTPUT VOLTAGE : 2.5 to 36V
- SINK CURRENT CAPABILITY : 1 to 100mA
- TYPICAL OUTPUT IMPEDANCE : 0.22Ω
- 1% AND 2% VOLTAGE PRECISION

Z
TO92
(Plastic Package)



D
SO8
(Batwing Plastic Micropackage)

DESCRIPTION

The TL431 is a programmable shunt voltage reference with guaranteed temperature stability over the entire temperature range of operation.

The output voltage may be set to any value between 2.5V and 36V with two external resistors.

The TL431 operates with a wide current range from 1 to 100mA with a typical dynamic impedance of 0.22Ω.

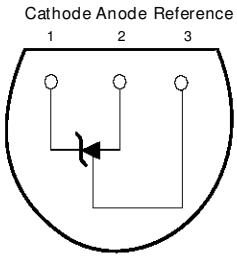
ORDER CODE

Part Number	Temperature Range	Package	
		Z	D
TL431C/AC	0°C, +70°C	•	•
TL431I/AI	-40°C, +105°C	•	•

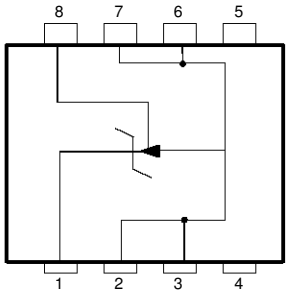
Z = TO92 Plastic package - also available in Bulk (Z), Tape & Reel (ZT) and Ammo Pack (AP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)

TO92
(Top view)



SO8
(Top view)



1- Cathode
2- Anode
3- Anode.
4- N.C.
5- N.C.
6- Anode
7- Anode.
8- Reference

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{KA}	Cathode to Anode Voltage	37	V
I_k	Continuous Cathode Current Range	-100 to +150	mA
I_{ref}	Reference Input Current Range	-0.05 to +10	mA
p_d	Power Dissipation [1] TO92 SO8 batwing	625 960	mW
T_{stg}	Storage Temperature Range	-65 to +150	°C

1. Pd is calculated with T_{amb} = +25°C, T_j = +150°C and R_{thja} = 200°C/W for TO92 package
= 130°C/W for SO8 batwing package

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{KA}	Cathode to Anode Voltage	V_{ref} to 36	V
I_k	Cathode Current	1 to 100	mA
T_{oper}	Operating Free-air Temperature Range TL431C/AC TL431I/AI	0 to +70 -40 to +105	°C

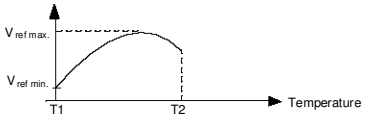
ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TL431C			TL431AC			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{ref}	Reference Input Voltage $V_{KA} = V_{ref}$, Ik = 10 mA T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	2.44 2.423	2.495	2.55 2.567	2.47 2.453	2.495	2.52 2.537	V
ΔV_{ref}	Reference Input Voltage Deviation Over-Temperature Range - note 1 V_{KA} = Vref, Ik = 10 mA, $T_{min} \le T_{amb} \le T_{max}$		3	17		3	15	mV
$\frac{\Delta Vref}{\Delta Vka}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage - (figure 2) Ik = 10mA ΔV_{KA} = 10V to Vref ΔV_{KA} = 36V to 10V		-1.4 -1	-2.7 -2		-1.4 -1	-2.7 -2	mV/V
I_{ref}	Reference Input Current Ik = 10mA, R1 = 10kΩ, R2 = ∞ T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		1.8	4 5.2		1.8	4 5.2	µA
ΔI_{ref}	Reference Input Current Deviation Over Temperature Range Ik = 10mA, R1 = 10kΩ, R2 =∞ $T_{min} \le T_{amb} \le T_{max}$		0.4	1.2		0.4	1.2	µA
I_{min}	Minimum Cathode Current for Regulation $V_{KA} = V_{ref}$		0.5	1		0.5	0.6	mA
I_{off}	Off-State Cathode Current		2.6	1000		2.6	1000	nA
$\lvert Z_{KA} \rvert$	Dynamic Impedance - note 2 $V_{KA} = V_{ref}$, Δ Ik = 1 to100mA, f ≤1kHZ		0.22	0.5		0.22	0.5	Ω

1) ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full temperature range.

$\Delta V_{ref} = V_{ref\ max.} - V_{ref\ min.}$



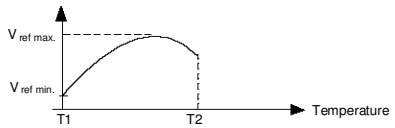
2) The dynamic Impedance is definied as $\lvert Z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_K}$

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	TL431I			TL431AI			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{ref}	Reference Input Voltage $V_{KA} = V_{ref}$, Ik = 10 mA T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	2.44 2.41	2.495	2.55 2.58	2.47 2.44	2.495	2.52 2.55	V
ΔV_{ref}	Reference Input Voltage Deviation Over-Temperature Range - note 1 $V_{KA} = V_{ref}$, Ik =10 mA, $T_{min} \le T_{amb} \le T_{max}$		7	30		7	30	mV
$\frac{\Delta Vref}{\Delta Vka}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage Ik = 10mA ΔV_{KA} = 10V to V_{ref} ΔV_{KA} = 36V to 10V		-1.4 -1	-2.7 -2		-1.4 -1	-2.7 -2	mV/V
Iref	Reference Input Current Ik = 10mA, R1 = 10kΩ, R2 = ∞ T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		1.8	4 6.5		1.8	4 6.5	µA
ΔIref	Reference Input Current Deviation Over Temperature Range Ik = 10mA, R1 = 10kΩ, R2 =∞ $T_{min} \le T_{amb} \le T_{max}$		0.8	2.5		0.8	1.2	µA
Imin	Minimum Cathode Current for Regulation $V_{KA} = V_{ref}$		0.5	1		0.5	0.7	mA
Ioff	Off-State Cathode Current		2.6	1000		2.6	1000	nA
$\lvert Z_{KA} \rvert$	Dynamic Impedance note 2 $V_{KA} = V_{ref}$,Δ Ik = 1 to100mA, f ≤1kHZ		0.22	0.5		0.22	0.5	Ω

1) ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full temperature range.
$\Delta V_{ref} = V_{ref\ max.} - V_{ref\ min.}$



2) The dynamic Impedance is definied as $\lvert Z_{KA} \rvert = \frac{\Delta V_{KA}}{\Delta I_K}$

Figure 1 : Test Circuit for $V_{KA} = V_{REF}$

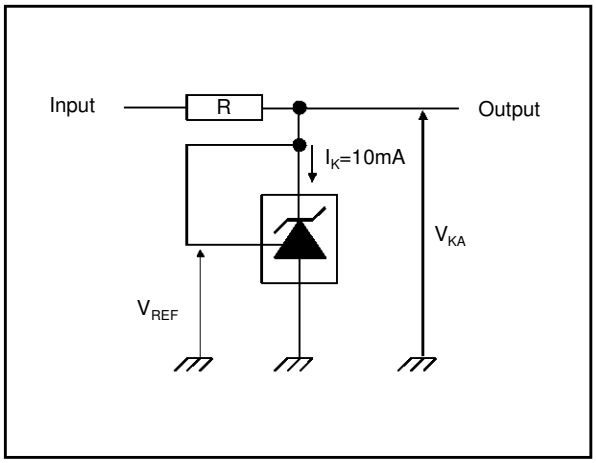


Figure 2 : Test Circuit for $V_{KA} > V_{REF}$

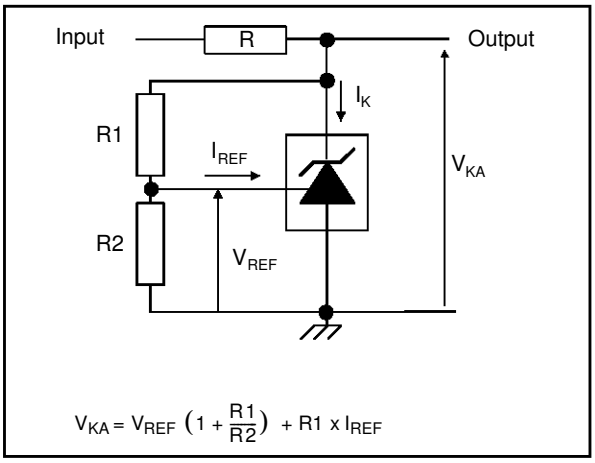


Figure 3 : Test Circuit for I_{OFF}

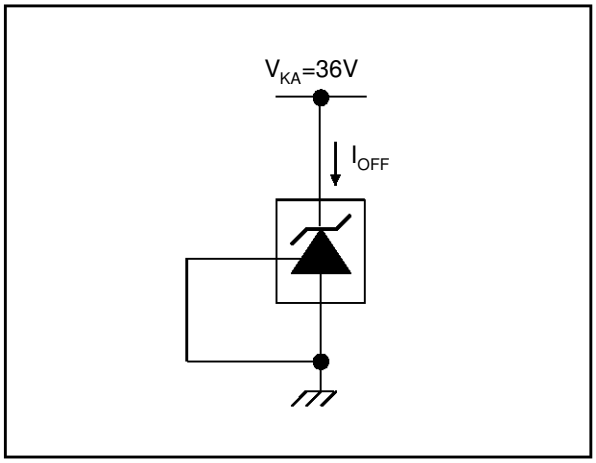


Figure 4 : Test Circuit for Phase Margin and Voltage Gain

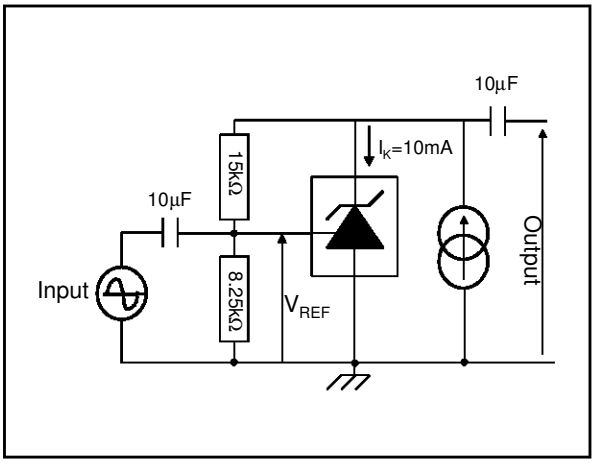


Figure 5 : Block diagram of TL1431

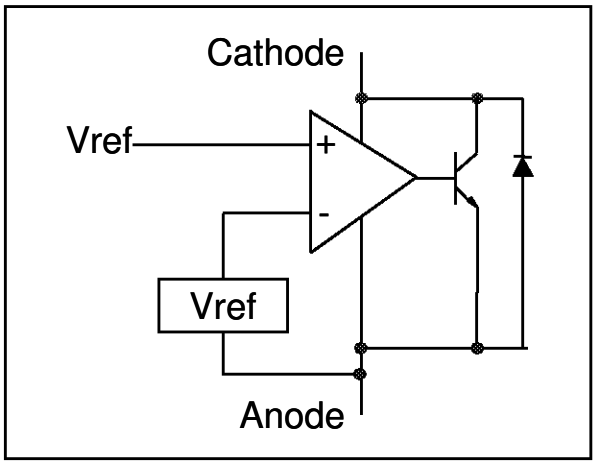
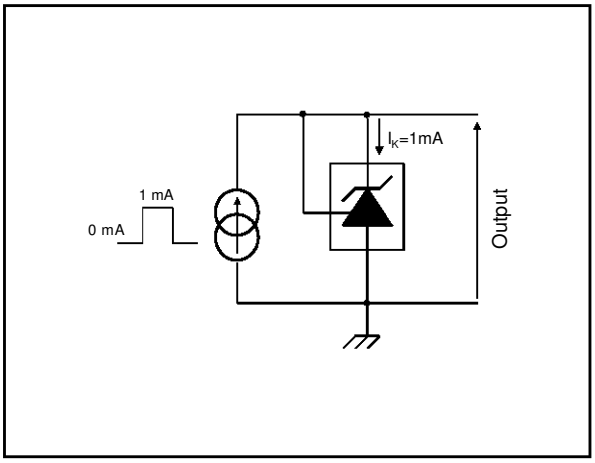


Figure 6 : Test Circuit for Response time



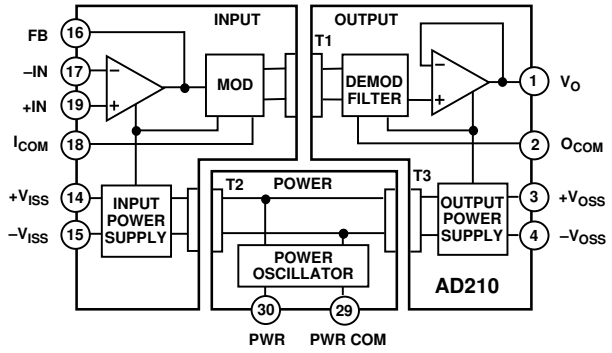
Precision, Wide Bandwidth 3-Port Isolation Amplifier

AD210*

FEATURES
High CMV Isolation: 2500 V rms Continuous
±3500 V Peak Continuous
Small Size: 1.00" × 2.10" × 0.350"
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20 kHz Full-Power (–3 dB)
Low Gain Drift: ±25 ppm/°C max
High CMR: 120 dB (G = 100 V/V)
Isolated Power: ±15 V @ ±5 mA
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD210 is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15 V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multichannel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may other vise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500 V rms (Continuous) and ± 3500 V peak (Continuous) common-mode voltage isolation between any two ports. Low input capacitance of 5 pF results in a 120 dB CMR at a gain of 100, and a low leakage current (2 μA rms max @ 240 V rms, 60 Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ±25 ppm/°C max and input offset drift of (±10 ±30/G) μV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20 kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00" × 2.10" × 0.350". The low profile DIP package allows application in 0.5" card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15 V @ 5 mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required and facilitates many alternative input functions as required by the user.

***Covered by U.S. Patent No. 4,703,283.**

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

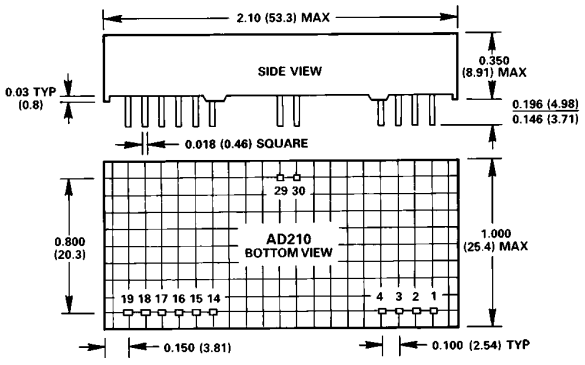
AD210–SPECIFICATIONS (typical @ +25°C, and V_S = +15 V unless otherwise noted)

Model	AD210AN	AD210BN	AD210JN
GAIN			
Range	1 V/V – 100 V/V	*	*
Error	±2% max	±1% max	*
vs. Temperature(0°C to +70°C)	+25 ppm/°C max	*	*
(–25°C to +85°C)	±50 ppm/°C max	*	*
vs. Supply Voltage	±0.002%/V	*	*
Nonlinearity[1]	±0.025% max	±0.012% max	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10 V	*	*
Maximum Safe Differential Input	±15 V	*	*
Max. CMV Input-to-Output	*		
ac, 60 Hz, Continuous	2500 V rms	*	1500 V rms
dc, Continuous	±3500 V peak	*	±2000 V peak
Common-Mode Rejection	*		
60 Hz, G = 100 V/V	*		
$R_S \leq 500\ \Omega$ Impedance Imbalance	120 dB	*	*
Leakage Current Input-to-Output	*		
@ 240 V rms, 60 Hz	2 µA rms max	*	*
INPUT IMPEDANCE			
Differential	$10^{12}\ \Omega$	*	*
Common Mode	5 GΩ‖5 pF	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	30 pA typ (400 pA max)	*	*
vs. Temperature (0°C to +70°C)	10 nA max	*	*
(–25°C to +85°C)	30 nA max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	5 pA typ (200 pA max)	*	*
vs. Temperature(0°C to + 70°C)	2 nA max	*	*
(–25°C to +85°C)	10 nA max	*	*
INPUT NOISE			
Voltage (1 kHz)	18 nV/√Hz	*	*
(10 Hz to 10 kHz)	4 µV rms	*	*
Current (1 kHz)	0.01 pA/√Hz	*	*
FREQUENCY RESPONSE			
Bandwidth (–3 dB)	*		
G = 1 V/V	20 kHz	*	*
G = 100 V/V	15 kHz	*	*
Settling Time (±10 mV, 20 V Step)	*		
G = 1 V/V	150 µs	*	*
G = 100 V/V	500 µs	*	*
Slew Rate (G = 1 V/V)	1 V/µs	*	*
OFFSET VOLTAGE (RTI)[2]			
Initial, @ +25°C	±15 ±45/G) mV max	(±5 ±15/G) mV max	*
vs. Temperature (0°C to +70°C)	(±10 ±30/G) µV/°C	*	*
(–25°C to +85°C)	(±10 ±50/G) µV/°C	*	*
RATED OUTPUT[3]			
Voltage, 2 kΩ Load	±10 V min	*	*
Impedance	1 Ω max	*	*
Ripple (Bandwidth = 100 kHz)	10 mV p-p max	*	*
ISOLATED POWER OUTPUTS[4]			
Voltage, No Load	±15 V	*	*
Accuracy	±10%	*	*
Current	±5 mA	*	*
Regulation, No Load to Full Load	See Text	*	*
Ripple	See Text	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15 V dc ± 5%	*	*
Voltage, Operating	+15 V dc ± 10%	*	*
Current, Quiescent	50 mA	*	*
Current, Full Load – Full Signal	80 mA	*	*
TEMPERATURE RANGE			
Rated Performance	–25°C to +85°C	*	*
Operating	–40°C to +85°C	*	*
Storage	–40°C to +85°C	*	*
PACKAGE DIMENSIONS			
Inches	1.00 × 2.10 × 0.350	*	*
Millimeters	25.4 × 53.3 × 8.9	*	*

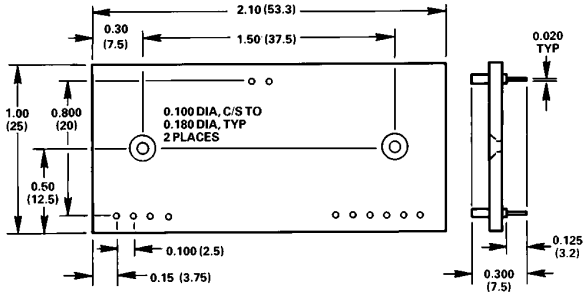
NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line..
[2]RTI – Referred to Input.
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 MATING SOCKET



AD210 PIN DESIGNATIONS

Pin	Designation	Function
1	V_O	Output
2	O_{COM}	Output Common
3	$+V_{OSS}$	+Isolated Power @ Output
4	$–V_{OSS}$	–Isolated Power @ Output
14	$+V_{ISS}$	+Isolated Power @ Input
15	$–V_{ISS}$	–Isolated Power @ Input
16	FB	Input Feedback
17	–IN	–Input
18	I_{COM}	Input Common
19	+IN	+Input
29	Pwr Com	Power Common
30	Pwr	Power Input

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD210 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

INSIDE THE AD210

The AD210 basic block diagram is illustrated in Figure 1. A +15 V supply is connected to the power port, and ±15 V isolated power is supplied to both the input and output ports via a 50 kHz carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The fullwave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A 20 kHz, three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a 2 kΩ load.

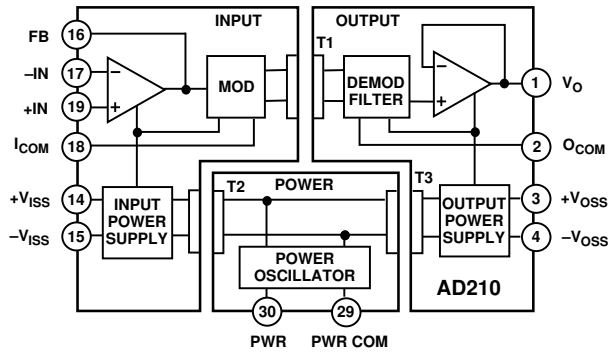


Figure 1. AD210 Block Diagram

USING THE AD210

The AD210 is very simple to apply in a wide range of applications. Powered by a single +15 V power supply, the AD210 will provide outstanding performance when used as an input or output isolator, in single and multichannel configurations.

Input Configurations: The basic unity gain configuration for signals up to ±10 V is shown in Figure 2. Additional input amplifier variations are shown in the following figures. For smaller signal levels Figure 3 shows how to obtain gain while maintaining a very high input impedance.

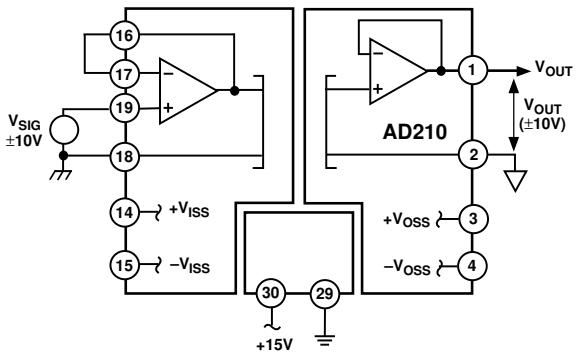


Figure 2. Basic Unity Gain Configuration

The high input impedance of the circuits in Figures 2 and 3 can be maintained in an inverting application. Since the AD210 is a three-port isolator, either the input leads or the output leads may be interchanged to create the signal inversion.

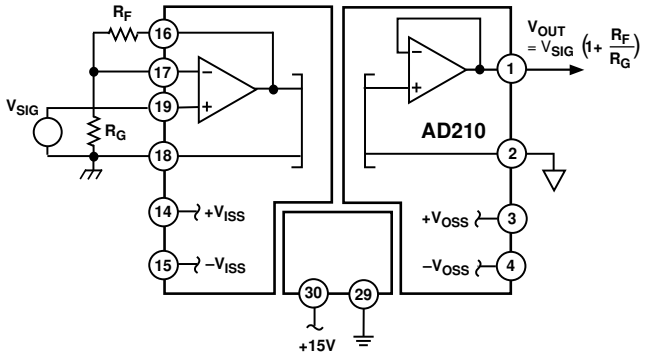


Figure 3. Input Configuration for G > 1

Figure 4 shows how to accommodate current inputs or sum currents or voltages. This circuit configuration can also be used for signals greater than ±10 V. For example, a ±100 V input span can be handled with R_F = 20 kΩ and R_{S1} = 200 kΩ.

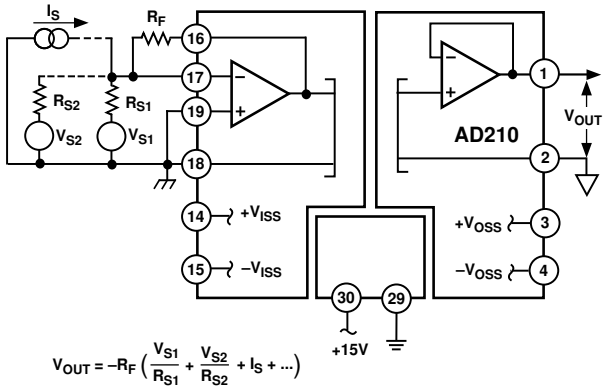


Figure 4. Summing or Current Input Configuration

Adjustments

When gain and offset adjustments are required, the actual circuit adjustment components will depend on the choice of input configuration and whether the adjustments are to be made at the isolator's input or output. Adjustments on the output side might be used when potentiometers on the input side would represent a hazard due to the presence of high common-mode voltage during adjustment. Offset adjustments are best done at the input side, as it is better to null the offset ahead of the gain.

Figure 5 shows the input adjustment circuit for use when the input amplifier is configured in the noninverting mode. This offset adjustment circuit injects a small voltage in series with the

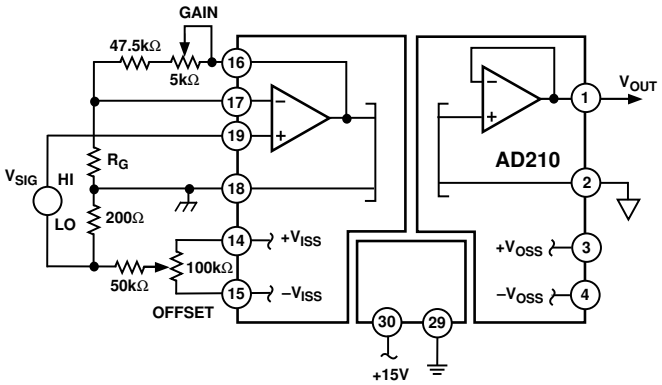


Figure 5. Adjustments for Noninverting Input

On-Board Type (DC) EMI Suppression Filters (EMIFIL®)

Block Type EMIFIL® BNX Series

BNX Series

The block type "EMIFIL" BNX series incorporates through-type capacitor, monolithic chip capacitors and bead. The BNX is high performance for use in DC power circuits.

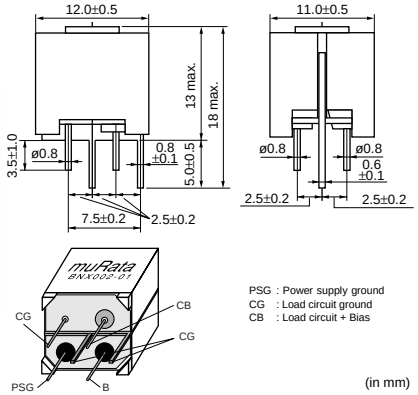
■ Features

1. The filter enables obtaining high insertion loss in wide frequency ranges from 0.5MHz to 1GHz.
2. The only one filter block enable noise suppression of both the positive and negative lines.
3. There are no connection routes in the current circuits, thus ensuring highly reliable performance.

■ Applications

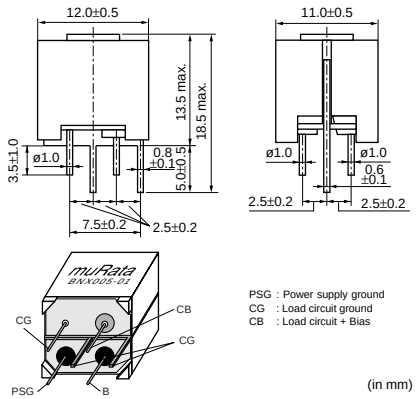
Noise suppression for DC power line of large screen display
1. PDP
2. LCD-TV

BNX002/BNX003



(in mm)

BNX005

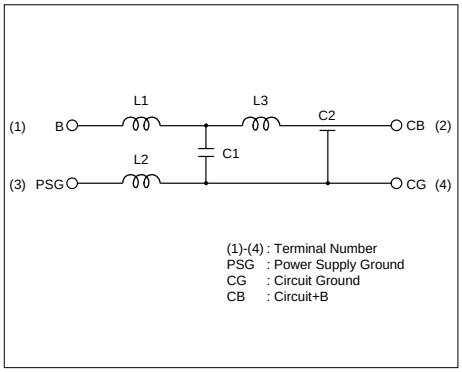


(in mm)

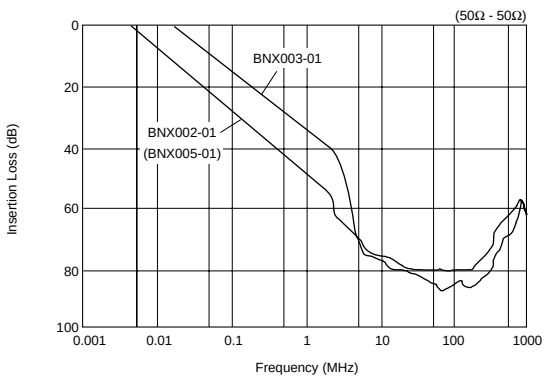
Part Number	Rated Voltage (Vdc)	Withstand Voltage (Vdc)	Rated Current (A)	Insulation Resistance (min.) (M ohm)	Insertion Loss
BNX002-01	50	125	10	100	1MHz to 1GHz:40dB min.(20 to 25°C line impedance=50 ohm)
BNX003-01	150	375	10	100	5MHz to 1GHz:40dB min.(20 to 25°C line impedance=50 ohm)
BNX005-01	50	125	15	100	1MHz to 1GHz:40dB min.(20 to 25°C line impedance=50 ohm)

Operating Temperature Range : -30°C to 85°C

■ Equivalent Circuit



■ Insertion Loss Characteristics (Typical)

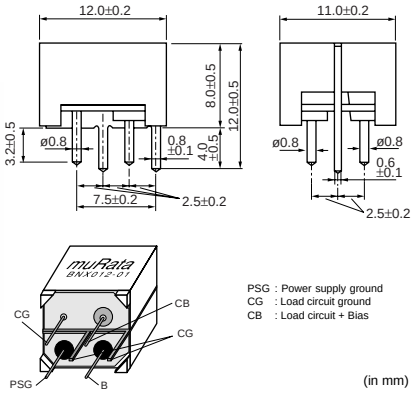


4

BNX Series Low Profile for Large Current

The block type "EMIFIL" BNX010 series is high performance and BNX series provide excellent noise suppression on DC power line.

BNX012



■ Features

1. High insertion loss characteristic over a wide frequency band range of 1MHz to 1GHz
2. Large rated current (15A) and Low Rdc (0.8m ohm-typ.)
3. Low profile (height: 8.0mm except lead terminal)

■ Applications

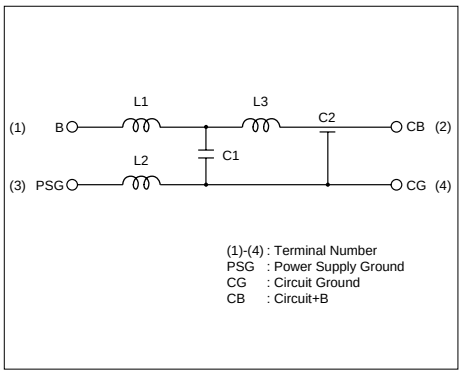
Noise suppression for DC power line of large screen display

1. PDP
2. LCD-TV

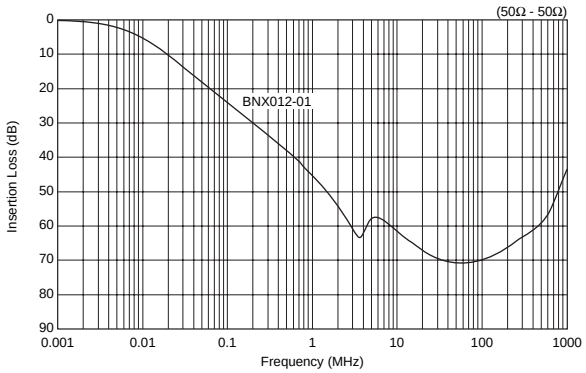
Part Number	Rated Voltage (Vdc)	Withstand Voltage (Vdc)	Rated Current (A)	Insulation Resistance (min.) (M ohm)	Insertion Loss
BNX012-01	50	125	15	500	1MHz to 1GHz:40dB min.(20 to 25°C line impedance=50 ohm)

Operating Temperature Range : -40°C to 125°C

■ Equivalent Circuit

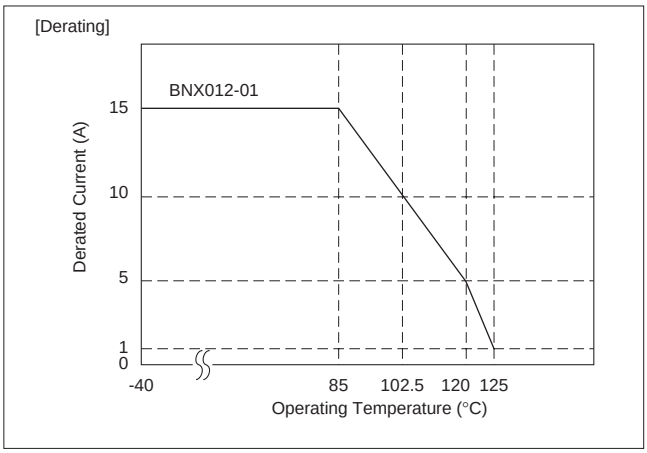


■ Insertion Loss Characteristics (Typical)



■ Notice (Rating)

In operating temperatures exceeding +85°C, derating of current is necessary for BNX010 series. Please apply the derating curve shown in chart according to the operating temperature.



Data sheet acquired from Harris Semiconductor
SCHS047D

August 1998 - Revised March 2000

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to $20V_{P-P}$ can be achieved by digital signal amplitudes of 4.5V to 20V (if V_{DD}-V_{SS} = 3V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0V, and V_{EE} = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic “1” is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the “CHANNEL IN/OUT” terminals are the outputs and the “COMMON OUT/IN” terminals are the inputs.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BNS	-55 to 125	16 Ld SOIC
CD4051BPW, CD4052BPW, CD4053BPW	-55 to 125	16 Ld TSSOP

Features

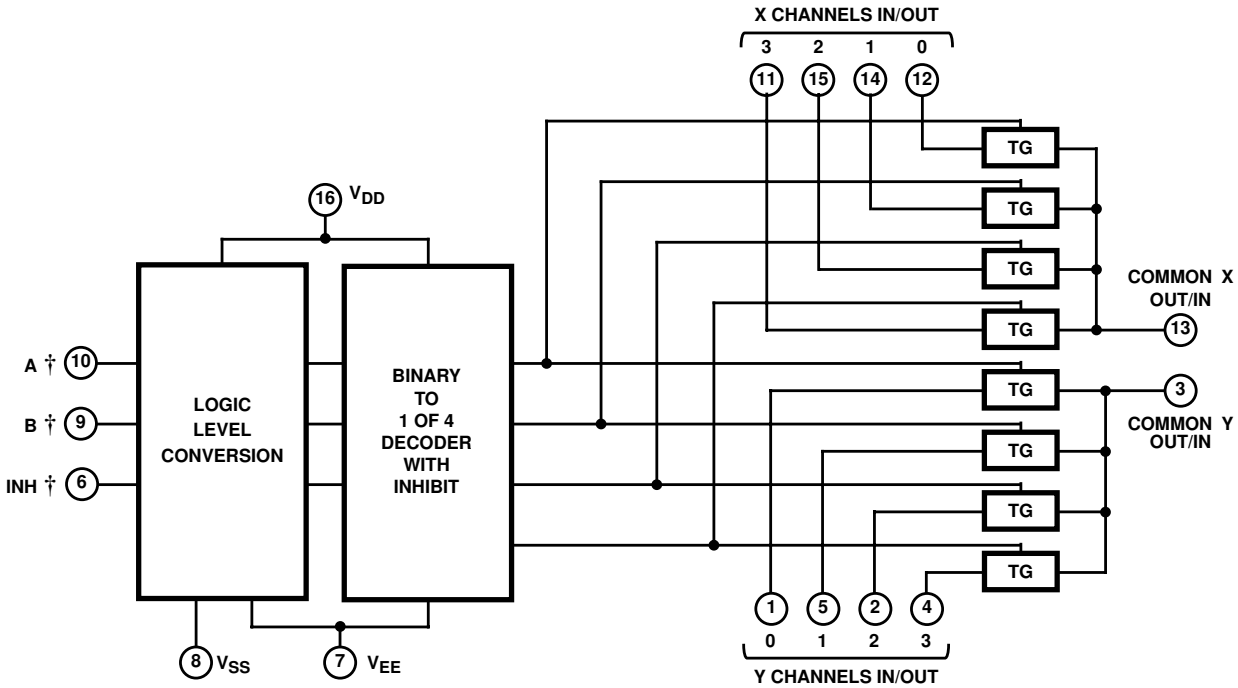
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . $\leq 20V_{P-P}$
- Low ON Resistance, 125Ω (Typ) Over $15V_{P-P}$ Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to $20V_{P-P}$ (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25^{O}C
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

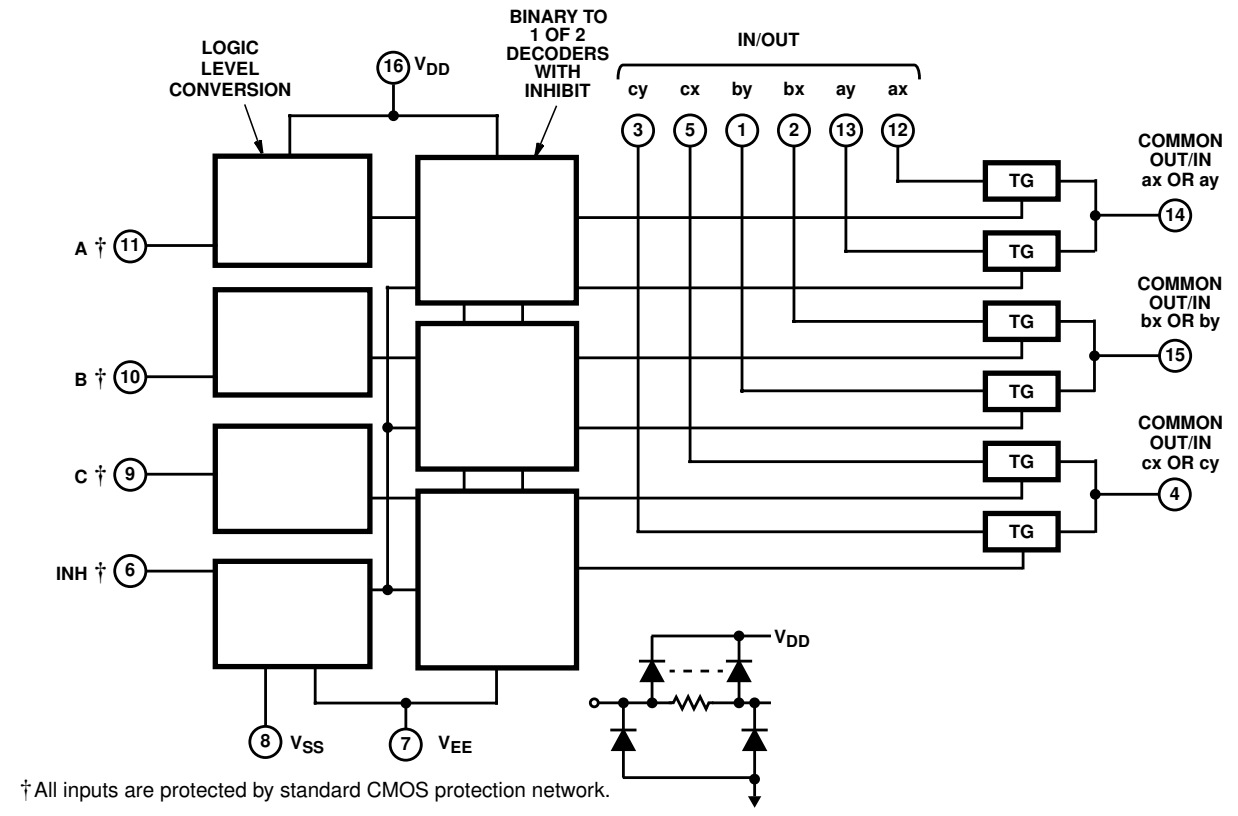
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

Functional Block Diagrams (Continued)

CD4052B



CD4053B



† All inputs are protected by standard CMOS protection network.

TRUTH TABLES

INPUT STATES				
INHIBIT	**C**	**B**	**A**	**"ON" CHANNEL(S)**
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
INHIBIT	**B**		**A**	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
CD4053B				
INHIBIT	**A OR B OR C**			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

X = Don't Care