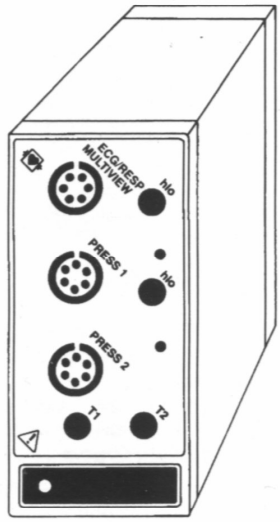
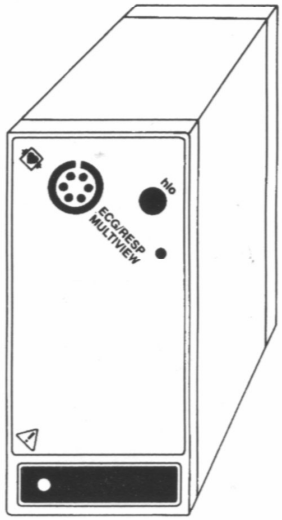
DOCUMENTATION

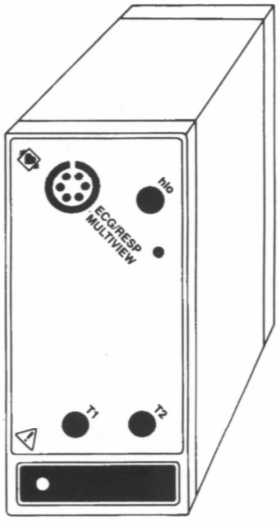
SpaceLabs Medical
The Clinical Information Company



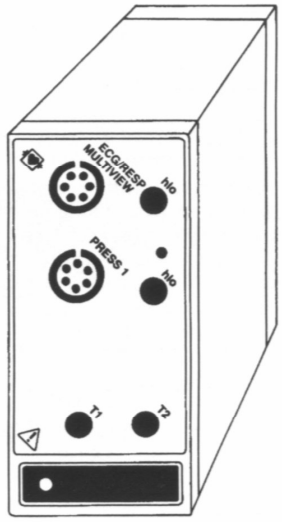
90470



90470-01



90470-02



90470-06

Integrated Multi-Parameter Modules 90470 90470-01 90470-02 90470-06

- **Touchscreen control of all module functions and compatible with all Patient Care Monitoring System (PCMS™) monitors**
- **Module Configuration Manager allows hospital to customize module function to specific patient populations, clinical protocols or operating preferences**
- **Multi-lead ECG with comprehensive arrhythmia and ST analysis and trending options**
- **Graded alarm function allows the hospital to define different alarm tones (i.e., high, medium or low) according to event severity (critical, warning, advisory)**
- **Automatic detection of ECG lead fault with user notification; selectable automatic lead switching to maintain monitoring continuity**
- **Adult and neonatal algorithms**

SPECIFICATIONS

Module Configurations —

90470 - Multi-lead ECG, invasive pressure (2 channels), temperature (2 channels)

90470-01 - Multi-lead ECG

90470-02 - Multi-lead ECG, temperature (2 channels)

90470-06 - Multi-lead ECG; invasive pressure (1 channel), temperature (2 channels)

All modules include:

— **Module Configuration Manager** capability (see the *Module Configuration Manager* chapter of the *PCMS Operations Manual* or the *UCW Operations Manual* for complete feature specifications)

— **Basic ECG** alarms for high and low heart rate, asystole and ventricular fibrillation

— **ESIS**

— **Trends** — (with appropriate mainframe option) 24 hours of trended data can be

Integrated Multi-Parameter Modules
90470
90470-01
90470-02
90470-06

SPECIFICATIONS

Data Shuttle™ — (Requires PCMS Monitor Option 20 or UCW Option Q) Includes data transfer features above, plus provides transfer for up to 24 hours of the database of the monitor, including continuous and episodic events, and trend information for all parameters monitored including modules and Flexport® interfaces

Please refer to the appropriate specifications for specific module parameters

ECG

Input Connector — 5-lead or 3-lead ECG cable with AAMI-standard connector (both cables use 1kΩ ± 10% resistors in series with each electrode)

Maximum Input — ± 5 mV (± 10%)

DC Offset — Up to ± 300 mV with no more than 2% signal amplitude degradation

Overdrive Recovery Time — < 1 second circuit settling time with offset voltage < 500 mV

Noise — 30 µV peak-to-peak (RTI) at 100 Hz bandwidth

CMRR — > 110 dB at line frequency (monitor mode) with patient cable and maximum 50 kΩ imbalance (referenced to chassis [earth] ground)

Pacer Rejection — Baseline shift < 0.2 mV (measured at ECG x 1,000 output)

Pacer Detection — Detects pacer pulses of ± 2 mV to ± 700 mV with pulse widths of 0.25 to 2 msec and rise times 10% of width not to exceed 100 µsec

Signal Bandwidth — 0.05 to 100 Hz ± 10% (-3 dB)

Display Bandwidth — 2 settings: 0.5 to 40 Hz ± 10% (-3 dB) in monitor mode, and 0.05 to 70 Hz ± 25% (-3 dB at 50 mm/sec) in extended mode

Sample Rate — 448 Hz

QRS Detection — Performed on up to 2 leads simultaneously; detects QRS complexes with durations of 20 to 120 ms and amplitudes of 0.2 to 5.0 mV (adult) or 0.15 to 5.0 mV (neonatal)

Abnormal Per Minute Counter — Displays counts up to 99 beats per minute

Heart Rate Range — 30 to 300 bpm; heart rates > 300 bpm are displayed as "+++"

Heart Rate Alarm Limits — High: 5 to 300 bpm, Low: 0 to 200 bpm; alarms automatically enabled over a range of 40 (adult) or 100 (neonatal) to 300 bpm

Accuracy — ± 1% or 2 beats per minute (whichever is greater)

Numeric Update Rate — Every 3 seconds or immediately at the onset of an alarm

Test Signal — 1 mV peak-to-peak (displayed via touchkey)

Display Size — Adjustable between 0.5 to 10 cm/mV; users can directly select a size of 1 cm/mV

Displayed Traces — 1 or 2; 2 traces require use of 5-lead patient cable

Trace Sweep Speeds — 50, 25, 12.5 mm per second

High Level Analog Input/Output (front panel) —
Used for defibrillator or intra-aortic balloon pump synchronization

Connector: 0.174" diameter, three conductor TT-phone plug

Dynamic Range: ± 5 mV (± 10%)

Gain: ECG x 1,000 (± 5%)

High Level Analog Output (back panel) — ECG and Pressure 1 (90470, 90470-06)

ECG and Respiration; if respiration is not available, second output is ECG (90470-01, 90470-02)

ST SEGMENT ANALYSIS

Signal Bandwidth — 0.05 to 100 Hz ± 10% (-3 dB) with mains frequency notch filter

ST Resolution — 8 µV/bit

ST Range — ± 9.20 mm (1 mV = 10 mm)

ST Alarms — Alarms for absolute minimum and maximum ST levels; also changes in ST level over the last 5 minutes

ST Displays — ST values; minimum/maximum/current ST segment deviation and 5-minute averaged segments for the last 30 minutes

ST Measurement Points — Adjustable ST, PR, and J points

ST Trends — Up to 24 hours of trend data can be displayed in 6-, 12- or 24-hour segments

RESPIRATION

Input Connector — 5-lead or 3-lead ECG cable with AAMI-standard connector (both cables use 1K Ω resistors (± 10%) in series with each electrode)

Measurement Technique — Impedance pneumography through ECG leads RA/LA, RL/LL, RL/LA, or RA/LL

Patient Source Impedance — 0 to 1,500 Ω at 62.5 kHz as measured at the patient cable branch

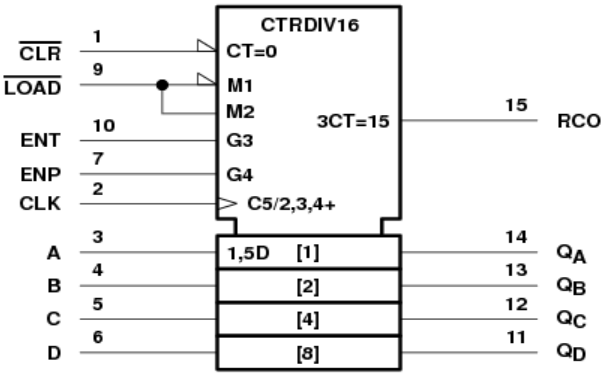
Excitation Frequency — 62.5 kHz (± 1%)

Excitation Amplitude — 80 µAmp (± 20%) RMS, 200 µAmp (± 20%) peak-to-peak

Noise — < 0.05 Ω peak-to-peak at 500 Ωs input source impedance

Signal Bandwidth —
Adult: 0.12 to 2.0 Hz (± 10%)
Neonate: 0.15 to 2.5 Hz (± 10%)

logic symbol†

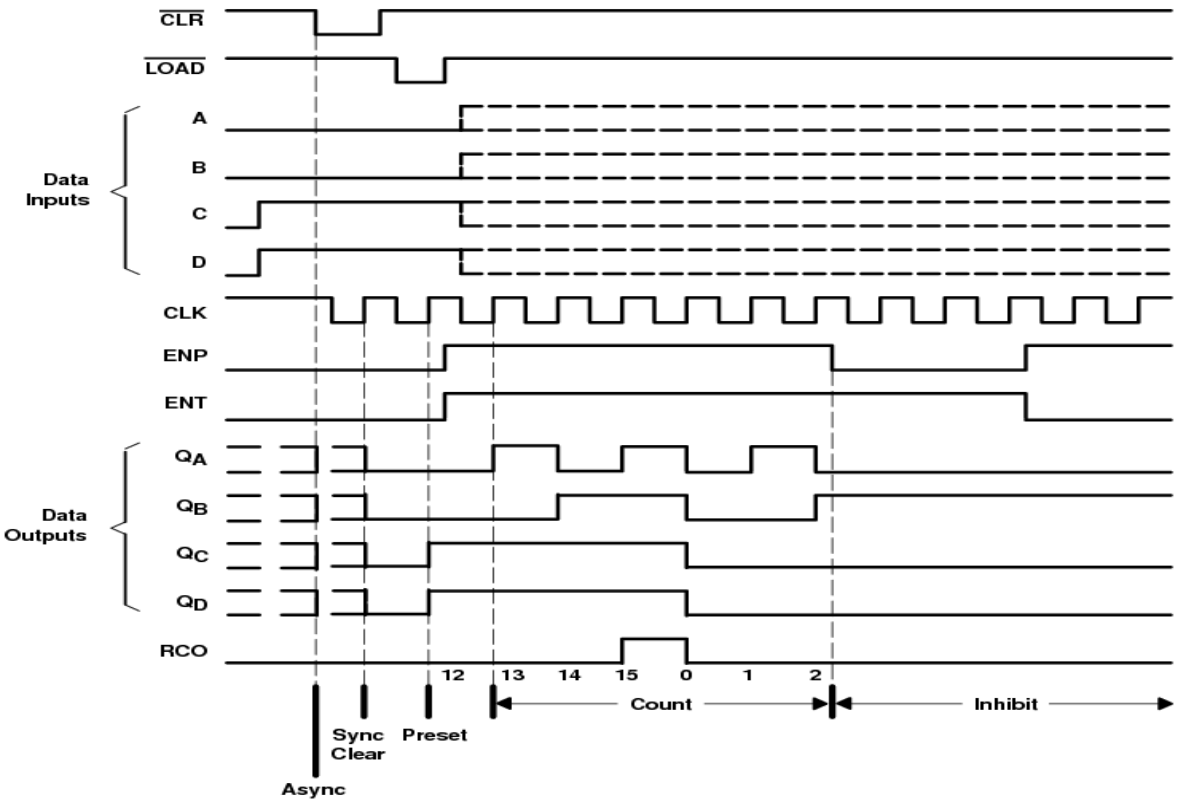


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS124D

January 1998 - Revised September 2003

CD54HC74, CD74HC74, CD54HCT74, CD74HCT74

Dual D Flip-Flop with Set and Reset Positive-Edge Trigger

Features

- **Hysteresis on Clock Inputs for Improved Noise Immunity and Increased Input Rise and Fall Times**
- **Asynchronous Set and Reset**
- **Complementary Outputs**
- **Buffered Inputs**
- **Typical f_{MAX} = 50MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**

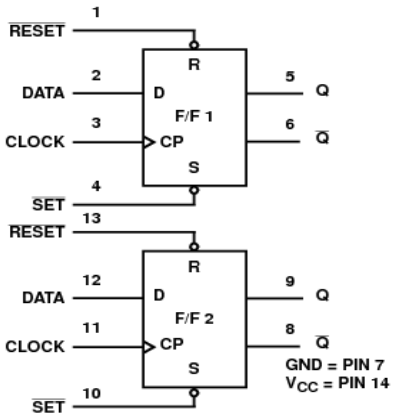
Description

The 'HC74 and 'HCT74 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The HCT logic family is functionally as well as pin compatible with the standard LS logic family.

Functional Diagram



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H= High Level (Steady State)
L= Low Level (Steady State)
X= Don't Care
↑= Low-to-High Transition
Q0 = the level of Q before the indicated input conditions were established.
NOTE:

1. This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

8-channel analogue multiplexer/demultiplexer

HEF4051B MSI

DESCRIPTION

The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs (A_0 to A_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by A_0 to A_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 to A_2.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 to A_2, and $\overline{E}$). The V_{DD} to V_{SS} range is 3 to 15 V.

The analogue inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

FUNCTION TABLE

INPUTS				CHANNEL ON
$\overline{E}$	A_2	A_1	A_0	
L	L	L	L	Y_0–Z
L	L	L	H	Y_1–Z
L	L	H	L	Y_2–Z
L	L	H	H	Y_3–Z
L	H	L	L	Y_4–Z
L	H	L	H	Y_5–Z
L	H	H	L	Y_6–Z
L	H	H	H	Y_7–Z
H	X	X	X	none

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial

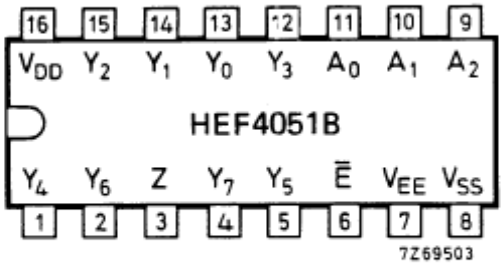


Fig.2 Pinning diagram.

LT1009, LT1009Y 2.5-V INTEGRATED REFERENCE CIRCUITS

description

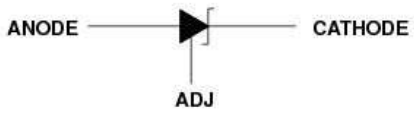
The LT1009 reference circuit is a precision-trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. A maximum initial tolerance of ±5 mV is available in the FK, JG, or LP package and ±10 mV in the D or PK package. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient α_{VZ}.

Even though the LT1009 needs no adjustments, a third terminal (ADJ) allows the reference voltage to be adjusted ±5% to eliminate system errors. In many applications, the LT1009 can be used as a terminal-for-terminal replacement for the LM136-2.5, which eliminates the external trim network.

The uses of the LT1009 include a 5-V system reference, an 8-bit ADC and DAC reference, and a power supply monitor. The LT1009 can also be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from −40°C to 85°C. The LT1009M is characterized for operation over the full military temperature range of −55°C to 125°C.

logic symbol



ANALOG DEVICES

LC²MOS Parallel Loading Dual 12-Bit DAC

AD7547

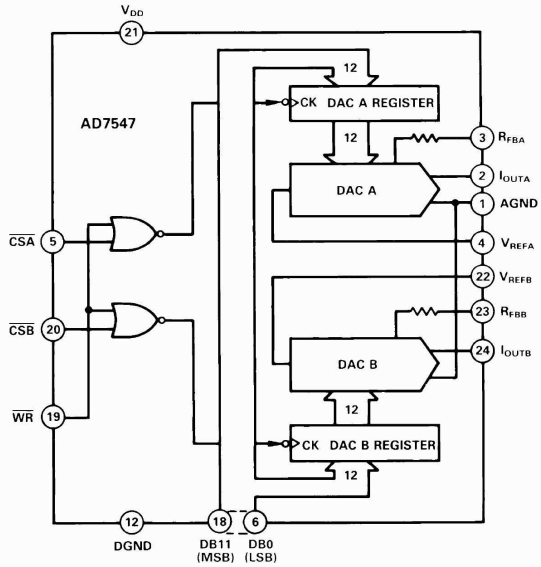
FEATURES
- Two 12-Bit DACs in One Package
- DAC Ladder Resistance Matching: 0.5%
- Space Saving Skinny DIP and Surface Mount Packages
- 4-Quadrant Multiplication
- Low Gain Error (1LSB max Over Temperature)
- Fast Interface Timing

GENERAL DESCRIPTION

The AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. $\overline{CSA}$, $\overline{CSB}$, $\overline{WR}$ control DAC selection and loading. Data is latched into the DAC registers on the rising edge of $\overline{WR}$. The device is speed compatible with most microprocessors and accepts TTL, 74HC and 5V CMOS logic level inputs.

The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. 12-bit monotonicity is guaranteed for both DACs over the full temperature range.

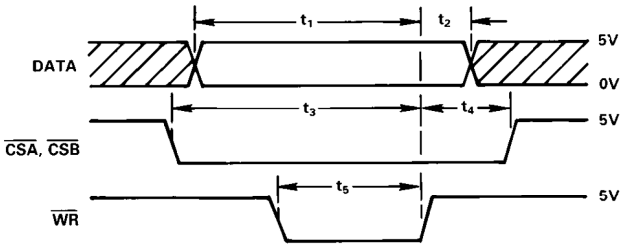
FUNCTIONAL BLOCK DIAGRAM



$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	FUNCTION
X	X	1	No Data Transfer
1	1	X	No Data Transfer
↓	↓	0	A Rising Edge on $\overline{CSA}$ or $\overline{CSB}$ Loads Data to the Respective DAC from the Data Bus
0	1	↓	DAC A Register Loaded from Data Bus
1	0	↓	DAC B Register Loaded from Data Bus
0	0	↓	DAC A and DAC B Registers Loaded from Data Bus

NOTES
1. X = Don't care
2. ↓ means rising edge triggered

Table I. AD7547 Truth Table



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH}+V_{IL}}{2}$

Figure 1. Timing Diagram for AD7547

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation.

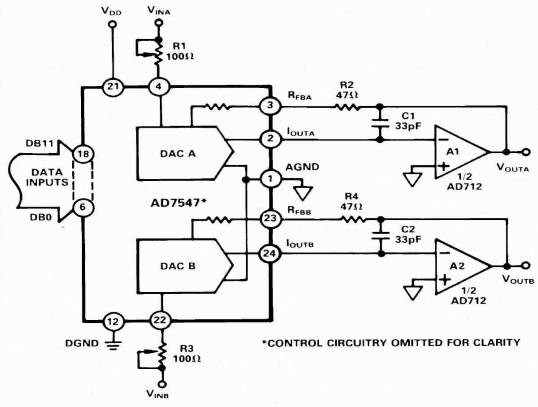


Figure 4. AD7547 Unipolar Binary Operation

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5.

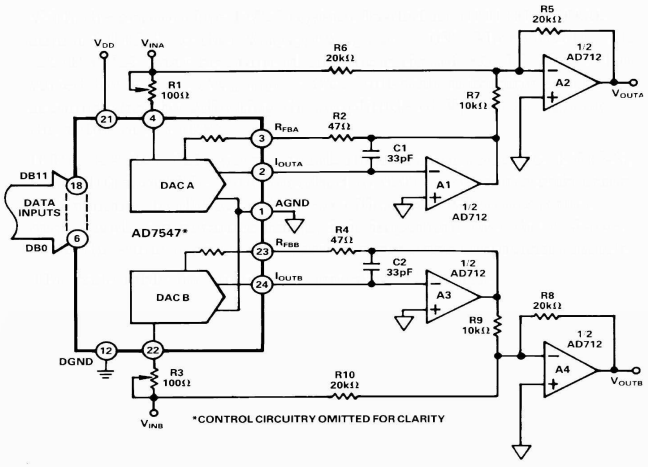
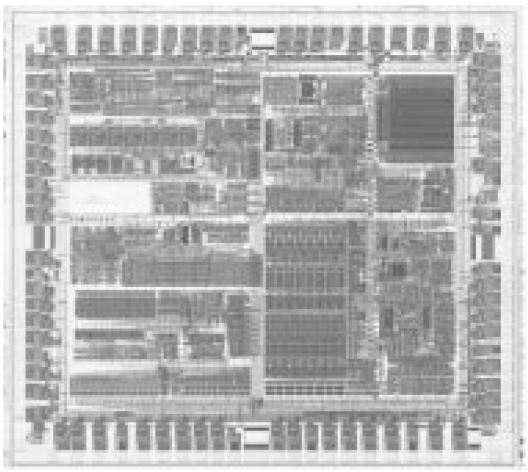


Figure 5. Bipolar Operation (Offset Binary Coding)

80C186XL/80C188XL
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSORS

- **Low Power, Fully Static Versions of 80C186/80C188**
- **Operation Modes:**
  - **— Enhanced Mode**
    - **— DRAM Refresh Control Unit**
    - **— Power-Save Mode**
    - **— Direct Interface to 80C187 (80C186XL Only)**
  - **— Compatible Mode**
    - **— NMOS 80186/80188 Pin-for-Pin Replacement for Non-Numerics Applications**
- **Integrated Feature Set**
  - **— Static, Modular CPU**
  - **— Clock Generator**
  - **— 2 Independent DMA Channels**
  - **— Programmable Interrupt Controller**
  - **— 3 Programmable 16-Bit Timers**
  - **— Dynamic RAM Refresh Control Unit**
  - **— Programmable Memory and Peripheral Chip Select Logic**
  - **— Programmable Wait State Generator**
  - **— Local Bus Controller**
  - **— Power-Save Mode**
  - **— System-Level Testing Support (High Impedance Test Mode)**
- **Completely Object Code Compatible with Existing 8086/8088 Software and Has 10 Additional Instructions over 8086/8088**
- **Speed Versions Available**
  - **— 25 MHz (80C186XL25/80C188XL25)**
  - **— 20 MHz (80C186XL20/80C188XL20)**
  - **— 12 MHz (80C186XL12/80C188XL12)**
- **Direct Addressing Capability to 1 MByte Memory and 64 Kbyte I/O**
- **Available in 68-Pin:**
  - **— Plastic Leaded Chip Carrier (PLCC)**
  - **— Ceramic Pin Grid Array (PGA)**
  - **— Ceramic Leadless Chip Carrier (JEDEC A Package)**
- **Available in 80-Pin:**
  - **— Quad Flat Pack (EIAJ)**
  - **— Shrink Quad Flat Pack (SGFP)**
- **Available in Extended Temperature Range (−40°C to +85°C)**

The Intel 80C186XL is a Modular Core re-implementation of the 80C186 microprocessor. It offers higher speed and lower power consumption than the standard 80C186 but maintains 100% clock-for-clock functional compatibility. Packaging and pinout are also identical.



272431-1

June, 2002 **Order Number: 272431-005**

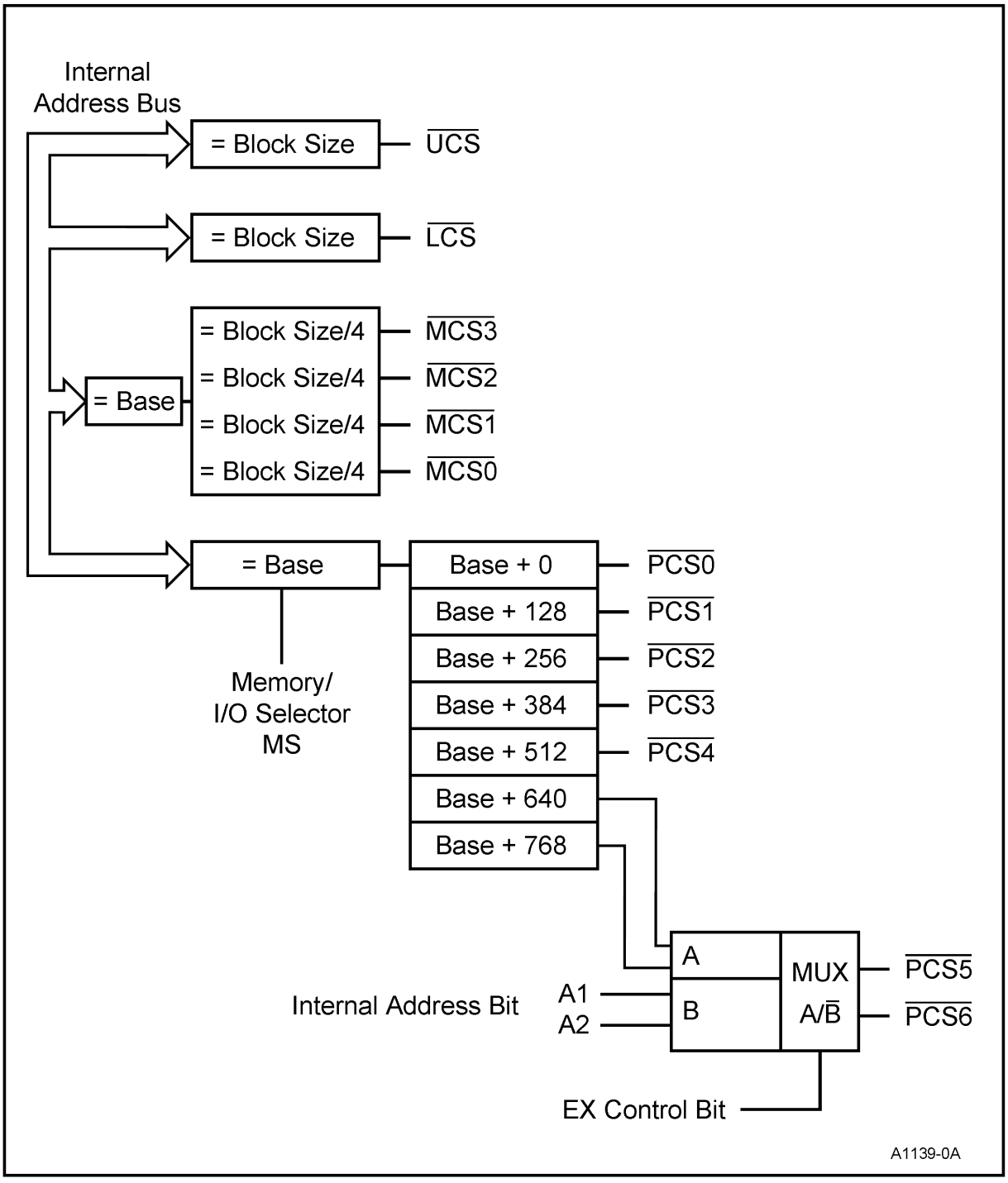


Figure 6-2. Chip-Select Block Diagram

$\overline{UCS}$ Mapped only to the upper memory address space; selects the BOOT memory device (EPROM or Flash memory types).

$\overline{LCS}$ Mapped only to the lower memory address space; selects a static memory (SRAM) device that stores the interrupt vector table, local stack, local data, and scratch pad data.

$\overline{MCS3:0}$ Mapped only to memory address space; selects additional SRAM memory, DRAM memory, or the system bus.

$\overline{PCS6:0}$ Mapped to memory or I/O address space; selects peripheral devices or generates a DMA acknowledge strobe. Note that each PCS*x* is not individually configurable for I/O space or memory space.

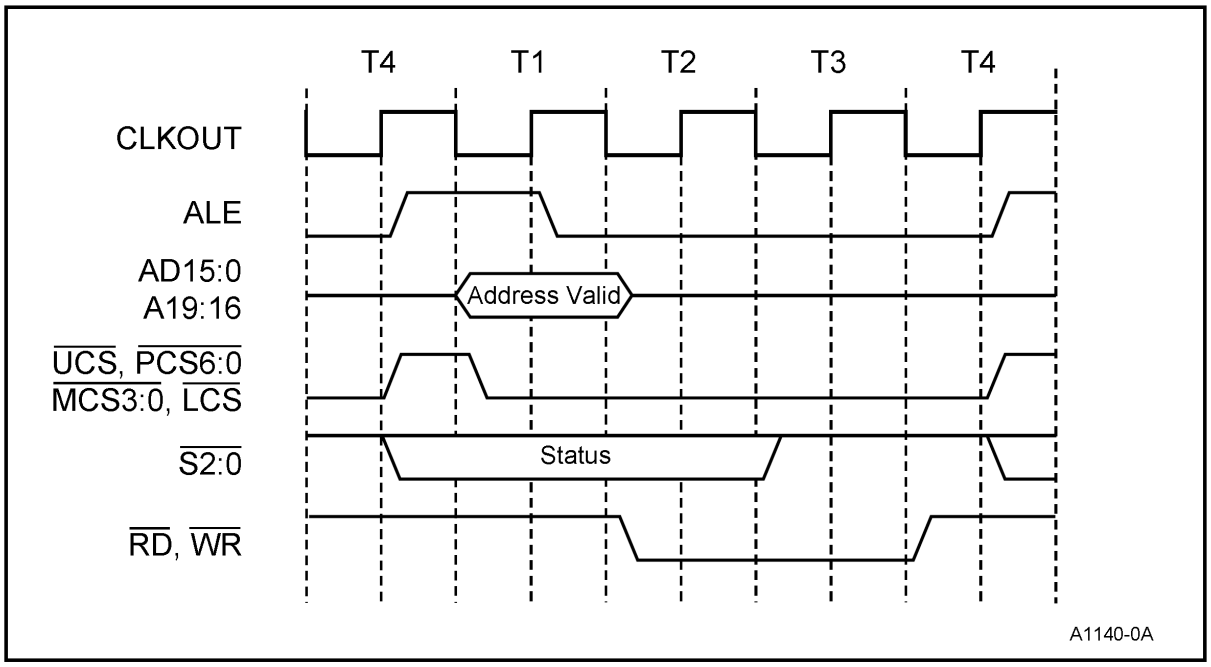


Figure 6-3. Chip-Select Relative Timings

The $\overline{UCS}$ chip-select always ends at address location 0FFFFH; its block size (and thus its starting address) is programmed in the UMCS register (Figure 6-5 on page 6-7). The $\overline{LCS}$ chip-select always starts at address location 0H; its block size (and thus its ending address) is programmed in the LMCS Control register (Figure 6-6 on page 6-8). The block size can range from 1 Kbyte to 256 Kbytes for both.

The $\overline{MCS3:0}$ chip-selects access a contiguous block of memory address space. The block size can range from 8 Kbytes to 512 Kbytes; it is programmed in the MMCS register (Figure 6-7 on page 6-9). Each chip-select goes active for one-fourth of the block. The start address is programmed in the MPCS register (Figure 6-9 on page 6-11); it must be an integer multiple of the block size. Because of the start address limitation, the $\overline{MCS3:0}$ chip-selects cannot cover the entire memory address space between the $\overline{LCS}$ and $\overline{UCS}$ chip-selects.

Table C-4. Instruction Set (Continued)

Name	Description	Operation	Flags Affected

MOV	**Move (Byte or Word):**
	MOV *dest, src*
	Transfers a byte or a word from the source operand to the destination operand.
	Instruction Operands:
	MOV mem, accum
	MOV accum, mem
	MOV reg, reg
	MOV reg, mem
	MOV mem, reg
	MOV reg, immed
	MOV mem, immed
	MOV seg-reg, reg16
	MOV seg-reg, mem16
	MOV reg16, seg-reg
	MOV mem16, seg-reg
		(dest)←(src)	AF –
			CF –
			DF –
			IF –
			OF –
			PF –
			SF –
			TF –
			ZF –

OUT	**Output:** OUT *port, accumulator* Transfers a byte or a word from the AL register or the AX register, respectively, to an output port. The port number may be specified either with an immediate byte constant, allowing access to ports numbered 0 through 255, or with a number previously placed in register DX, allowing variable access (by changing the value in DX) to ports numbered from 0 through 65,535. **Instruction Operands:** OUT immed8, AL OUT DX, AX	(dest) ← (src)	AF – CF – DF – IF – OF – PF – SF – TF – ZF –

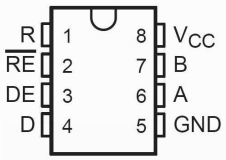
NOTE: The three symbols used in the Flags Affected column are defined as follows:
– the contents of the flag remain unchanged after the instruction is executed
? the contents of the flag is undefined after the instruction is executed
✓the flag is updated after the instruction is executed

Bitwise Operator Overview of the compilator

Operator	Operation	Operator	Operation
&	bitwise AND; compares pairs of bits and returns 1 if both bits are 1, otherwise returns 0	~	bitwise complement (unary); inverts each bit
|	bitwise (inclusive) OR; compares pairs of bits and returns 1 if either or both bits are 1, otherwise returns 0	<<	bitwise shift left; moves the bits to the left, discards the far left bit and assigns 0 to the right most bit.
^	bitwise exclusive OR (XOR); compares pairs of bits and returns 1 if the bits are complementary, otherwise returns 0	>>	bitwise shift right; moves the bits to the right, discards the far right bit and if unsigned assigns 0 to the left most bit, otherwise sign extends

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE
(TOP VIEW)



description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

Function Tables

DRIVER

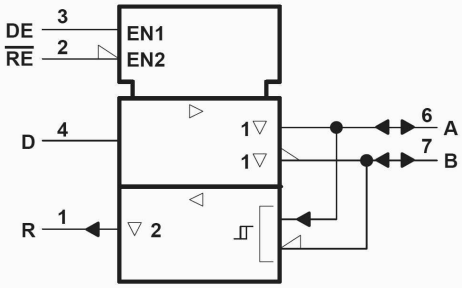
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

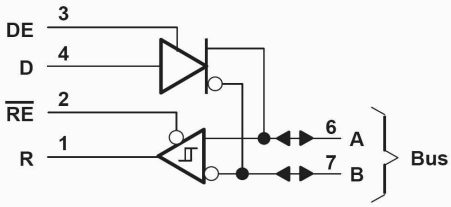
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Le protocole SDLC (Synchronous Data Link Control)

Ce protocole est destiné à des réseaux multi-périphériques, chaque périphérique étant repéré par une adresse unique.

Il est de type synchrone, l'horloge qui rythme l'émission des données est transmise sur un autre conducteur que les données.

Format de la trame SDLC

Une trame est une suite d'octets organisés en champs.

Longueur des champs en octet	**1**	**1**	**1**	**variable**	**2**	**1**
Nom des champs	**Drapeau**	**Adresse du destinataire**	**Commande**	**Données**	**FCS**	**Drapeau**

La partie utile (sans les drapeaux) de la trame SDLC a une longueur variable mais comprise entre 32 bits (4 octets) minimum et 1150 bits maximum. Cette partie utile est encadrée par des drapeaux qui indiquent le début et la fin de la trame.

Les différents champs sont toujours transmis poids faibles en premier, poids forts en dernier.

Contenu des différents champs

- Les **drapeaux** permettent au système de réception de reconnaître le début et la fin de la trame. Ils sont constitués de l'octet **01111110** (un 0 suivi de six 1 suivi d'un 0). Cela implique que dans le reste du message on ne pourra pas transmettre plus de cinq 1 consécutifs.

- Adresse du destinataire : contient l'adresse du périphérique auquel est destiné la commande ou les données

L'adresse « broadcast » $(11111111)_2$ ou $(FF)_{16}$ est utilisée pour transmettre un message à tous les périphériques.

- Commande : Ce champ indique le type de la trame (information, supervision ou non numéroté) et le numéro de la trame émise ou à recevoir.

- Données : Ce champ, lorsqu'il est présent, contient les données à transmettre entre les périphériques.Il peut être, lui-même, organisé à un niveau supérieur.

- Frame Check Sequence (FCS) : Ce champ permet au périphérique récepteur de détecter une erreur de transmission; il peut alors demander une retransmission des trames erronées.

Les bits de transparence

Pour qu'une succession de six 1 ne se produise que dans les drapeaux, on insère dans le reste de la trame un 0 après chaque suite de cinq 1. Ces bits supplémentaires sont éliminés par le récepteur.

Exemple : la portion de message 000111001111111000011111111111100000011 devient 000111001111**0**11000011111**0**11111**0**100000011 par insertion automatique des 0 notés en gras.

FEATURES

Form, Fit, and Function Compatible with the Intel® 8044/8344

Packaging options available: 40 Pin Plastic Dual In-Line Package (PDIP), 44 Pin Plastic Leaded Chip Carrier (PLCC)

8-Bit Control Unit

8-Bit Arithmetic-Logic Unit with 16-Bit multiplication and division

12 MHz clock

Four 8-Bit Input / Output ports

Two 16-Bit Timer/Counters

Serial Interface Unit with SDLC/HDLC compatibility

2.4 Mbps maximum serial data rate

Two Level Priority Interrupt System

5 Interrupt Sources

Internal Clock prescaler and Phase generator

192 Bytes of Read/Write Data Memory Space

64kB External Program Memory Space

64kB External Data Memory Space

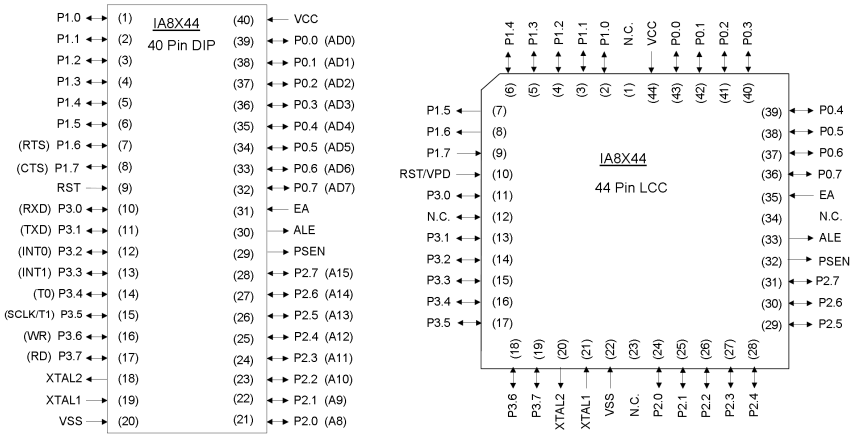
4kB Internal ROM (IA8044 only)

IA8044/IA8344 Variants

IA8044	4kB internal ROM with R0117 version 2.3 firmware, 192 byte internal RAM, 64kB external program and data space.
IA8344	192 byte internal RAM, 64kB external program and data space.

The IA8044/IA8344 is a "plug-and-play" drop-in replacement for the original IC. InnovASIC produces replacement ICs using its MILESTM, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILESTM captures the design of a clone so it can be produced even as silicon technology advances. MILESTM also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA8044/IA8344 including functional and I/O descriptions, electrical characteristics, and applicable timing.

Package Pinout



I/O Characteristics

The table below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provided. The table below provides the I/O description of the IA8044 and the IA8344.

Name	Type	Description
RST	I	Reset. This pin when held high for two machine cycles while the oscillator is running will cause the chip to reset.
ALE	O	Address Latch Enable. Used to latch the address on the falling edge for external memory accesses.
PSEN	O	Program Store Enable. When low acts as an output enable for external program memory.
EA	I	External Access. When held low EA will cause the IA8044/IA8344 to fetch instructions from external memory.
P0.7 – P0.0	I/O	Port 0. 8 bit I/O port and low order multiplexed address/data byte for external accesses.
P1.7 – P1.0	I/O	Port 1. 8-bit I/O port. Two bits have alternate functions, P1.6 (RTS) and P1.7 (CTS).
P2.7 – P2.0	I/O	Port 2. 8-bit I/O port. It also functions as the high order address byte during external accesses.
P3.7 – P3.0	I/O	Port 3. 8-bit I/O port. Port 3 bits also have alternate functions as described below. P3.0 – RXD. Receive data input for SIU or direction control for P3.1 dependent upon datalink configuration. P3.1 – TXD. Transmit data output for SIU or data input/output dependent upon datalink configuration. Also enables diagnostic mode when cleared. P3.2 – INT0. Interrupt 0 input or gate control input for counter 0. P3.3 – INT1. Interrupt 1 input or gate control input for counter 1. P3.4 – T0. Input to counter 0. P3.5 – SCLK/T1. SCLK input to SIU or input to counter 1. P3.6 – WR. External memory write signal. P3.7 – RD. External memory read signal.
XTAL1	I	Crystal Input 1. Connect to VSS when external clock is used on XTAL2. May be connected to a crystal (with XTAL2), or may be driven directly with a clock source (XTAL2 not connected).
XTAL2	O	Crystal Input 2. May be connected to a crystal (with XTAL1), or may be driven directly with an inverted clock source (XTAL1 tied to ground).
VSS	P	Ground.
VCC	P	+5V power.

Interrupts Vectors

Location	Service
0003H	External Interrupt 0
000BH	Timer 0 overflow
0013H	External Interrupt 1
001BH	Timer 1 overflow
0023H	SIU Interrupt

Timers/Counters

Timers 0 and 1

The IA8X44 has two 16-bit timer/counter registers: Timer 0 and Timer 1. Both can be configured for counter or timer operations. In timer mode, the register is incremented every machine cycle, which means that it counts up after every 12 oscillator periods. In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle (12 clock periods). Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

Mode 0

In mode 0 the timers operate as an 8-bit timer (TH0/1) with a divide by 32 bit prescalar (TL0/1). Mode 0 uses all 8 bits of TH0/1 and the lower 5 bits of TL0/1. The upper 3 bits of TL0/1 are unknowns. Setting TR0/1 does not reset the registers TH0/1 and TL0/1. As the timer rolls over from all 1's to all 0's it will set the interrupt flag TF0/1.

Mode 1

Mode 1 is the same as mode 0 except that all 8 bits of TL0/1 are used instead of just the lower 5 bits.

Mode 2

Mode 2 configures TL0/1 as an 8-bit counter with automatic reload from the contents of TH0/1. Overflow of TL0/1 causes the interrupt TF0/1 to be set and the reload to occur. The contents of TH0/1 are not affected by the reload.

Mode 3

Mode 3 creates two separate 8 bit counters from TL0 and TH0. TL0 uses the timer 0 mode bits from TMOD, TMOD.0 through TMOD.3. TH0 is a timer only (not a counter) and uses timer 1's control bits, TR1 and TF1 for operation. Timer 1 can still be used if an interrupt is not required by switching it in and out of its own mode 3. With TMOD.4 and TMOD.5 both high timer 1 will stop and hold its count.

Timer Mode (TMOD):

The Timer Mode register contains bits that select the mode that the timers are to be operated in. The lower nibble controls timer 0 and the upper nibble controls timer 1.

TMOD

Bit : 7	6	5	4	3	2	1	0
GATE	C/T	M1	M0	GATE	C/T	M1	M0

TMOD.0	M0	Timer 0 mode selector bit.
TMOD.1	M1	Timer 0 mode selector bit.
TMOD.2	C/T	C/T Selects Timer0 or Counter0 operation. When set to 1, the Counter operation is performed, when cleared to 0, the register will function as a Timer.
TMOD.3	GATE	If set, enables external gate control for counter/timer0 (pin INT0/ for Counter 0). When INT0/ is high, and TR0 bit is set (see TCON register), the counter is incremented every falling edge on T0 input pin.
TMOD.4	M0	Timer 1 mode selector bit.
TMOD.5	M1	Timer 1 mode selector bit.
TMOD.6	C/T	C/T Selects Timer1 or Counter1 operation. When set to 1, the Counter operation is performed, when cleared to 0, the register will function as a Timer.
TMOD.7	GATE	If set, enables external gate control for counter/timer1 (pin INT1/ for Counter 1). When INT1/ is high, and TR1 bit is set (see TCON register), the counter is incremented every falling edge on T1 input pin.

Timer Mode Select Bits

M1	M0	Operating Mode	
0	0	0	13 bit timer
0	1	1	16 bit timer/counter
1	0	2	8 bit auto-reload timer/counter
1	1	3	Timer0 – TL0 is a standard 8-bit timer/counter controlled by timer 0 control bits. TH0 is an 8-bit timer function only, controlled by timer 1 control bits.
1	1	3	Timer/counter1 stopped and holds its count. Can be used to start/stop timer 1 when timer 0 is in mode 3.

Timer Control (TCON):

The Timer Control register provides control bits that start and stop the counters. It also contains bits to select the type of external interrupt desired, edge or level. Additionally TCON contains status bits showing when a timer overflows and when an interrupt edge has been detected.

TCON

Bit : 7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TCON.0	IT0	Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.
TCON.1	IE0	Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT1/ is observed. Cleared when interrupt is processed.
TCON.2	IT1	Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.
TCON.3	IE1	Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1/ is observed Cleared when interrupt is processed.
TCON.4	TR0	Timer 0 Run control bit. If cleared, Timer 0 stops.
TCON.5	TF0	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag should be cleared by software.
TCON.6	TR1	Timer 1 Run control bit. If cleared, Timer 1 stops. In mode 3 this bit controls TH0.
TCON.7	TF1	Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag should be cleared by software.. In mode 3 this bit is controlled by TH0.

Timers/Counters Configuration

Timer 0 Mode 2