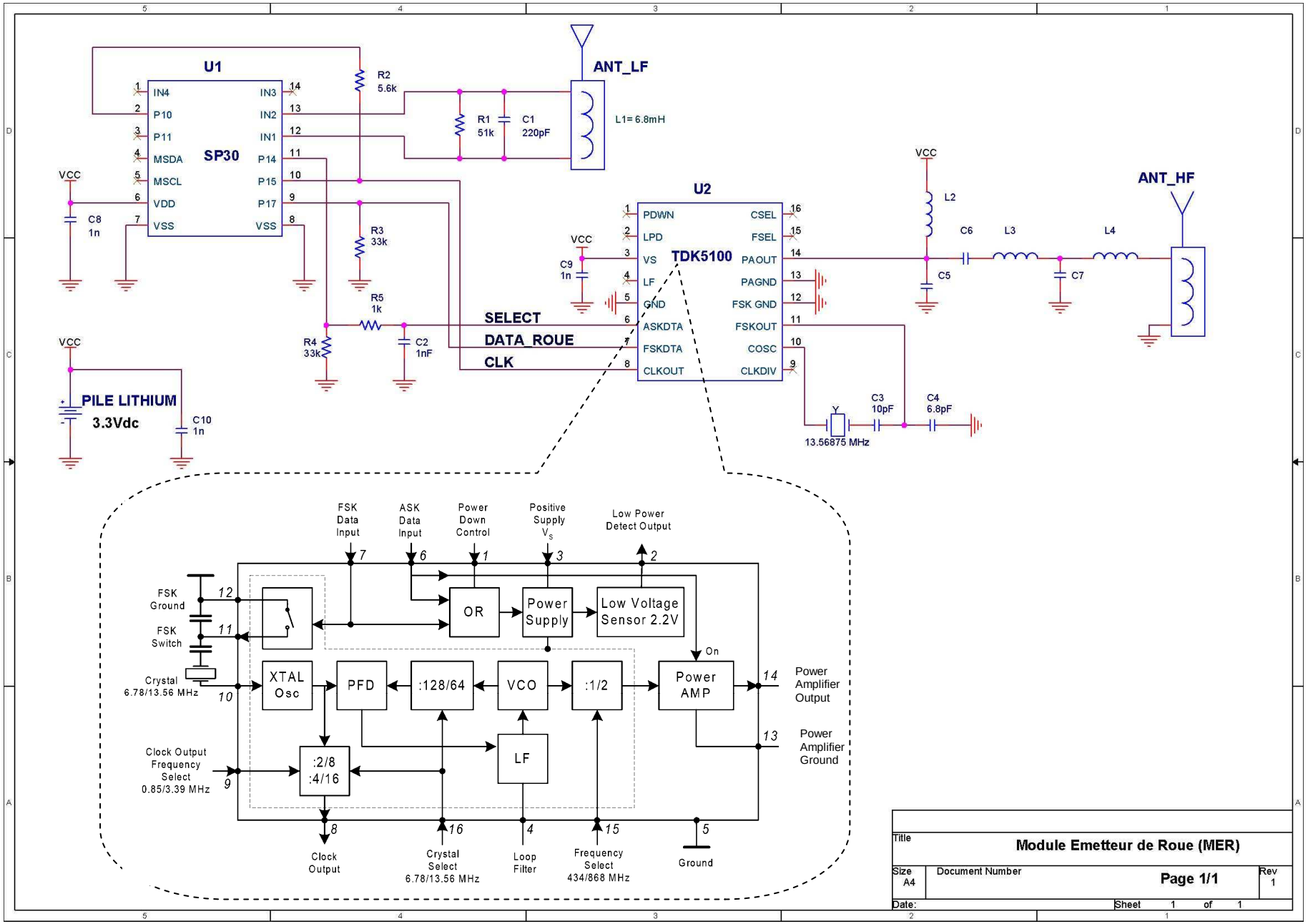
U1
SP30
IN4
P10
P11
MSDA
MSCL
VDD
VSS
IN3
IN2
IN1
P14
P15
P17
VSS
R2
5.6k
R1
51k
C1
220pF
ANT_LF
L1= 6.8mH
VCC
C8
1n
R3
33k
R5
1k
R4
33k
C2
1nF
SELECT
DATA_ROUE
CLK
U2
TDK5100
PDWN
LPD
VS
LF
GND
ASKDTA
FSKDTA
CLKOUT
CSEL
FSEL
PAOUT
PAGND
FSK GND
FSKOUT
COSC
CLKDIV
C9
1n
L2
C6
L3
L4
C5
C7
ANT_HF
PILE LITHIUM
3.3Vdc
C10
1n
Y
13.56875 MHz
C3
10pF
C4
6.8pF
FSK Data Input
ASK Data Input
Power Down Control
Positive Supply Vs
Low Power Detect Output
FSK Ground
FSK Switch
Crystal 6.78/13.56 MHz
OR
Power Supply
Low Voltage Sensor 2.2V
On
XTAL Osc
PFD
:128/64
VCO
:1/2
Power AMP
Power Amplifier Output
Power Amplifier Ground
Clock Output Frequency Select 0.85/3.39 MHz
:2/8
:4/16
LF
Clock Output
Crystal Select 6.78/13.56 MHz
Loop Filter
Frequency Select 434/868 MHz
Ground
Title
Module Emetteur de Roue (MER)
Size A4
Document Number
Page 1/1
Rev 1
Date:
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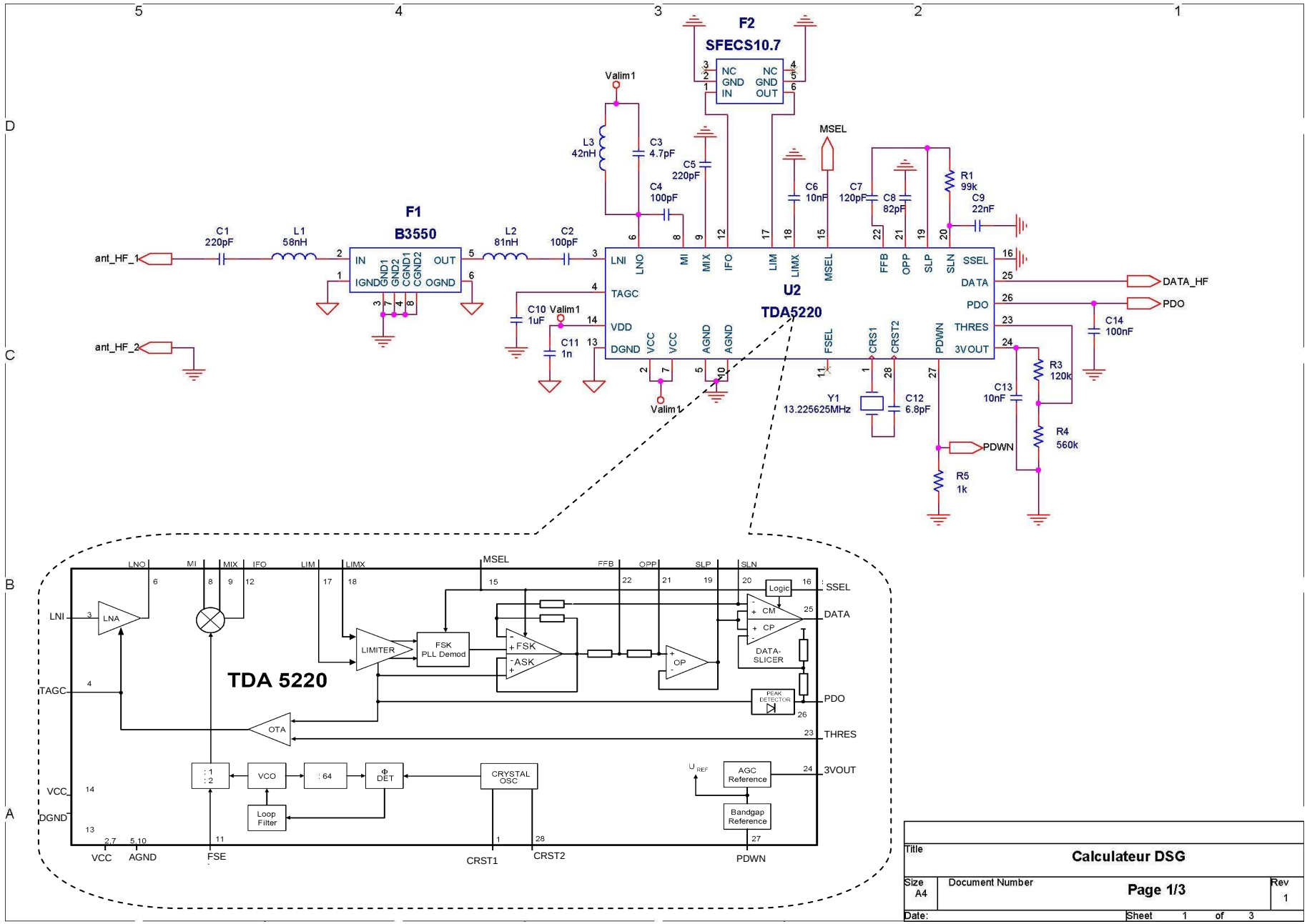
F2
SFECS10.7
NC
GND
IN
NC
GND
OUT
Valim1
L3
42nH
C3
4.7pF
C4
100pF
C5
220pF
MSEL
C6
10nF
C7
120pF
C8
82pF
R1
99k
C9
22nF
F1
B3550
C1
220pF
L1
58nH
L2
81nH
C2
100pF
ant_HF_1
ant_HF_2
IN
OUT
IGND
OGND
U2
TDA5220
LNI
LNO
MI
MIX
IFO
LIM
LIMX
MSEL
FFB
OPP
SLP
SLN
SSEL
DATA
PDO
THRES
3VOUT
TAGC
VDD
DGND
VCC
AGND
FSEL
CRS1
CRST2
PDWN
DATA_HF
PDO
C14
100nF
C10
1uF
C11
1n
R3
120k
C13
10nF
R4
560k
Y1
13.225625MHz
C12
6.8pF
PDWN
R5
1k
TDA 5220
LNA
LIMITER
FSK
PLL Demod
+ FSK
- ASK
OP
Logic
CM
CP
DATA-
SLICER
PEAK
DETECTOR
OTA
: 1
: 2
VCO
: 64
Φ
DET
CRYSTAL
OSC
Loop
Filter
U REF
AGC
Reference
Bandgap
Reference
VCC
DGND
AGND
FSE
CRST1
CRST2
PDWN
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Size
A4
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1
Date:
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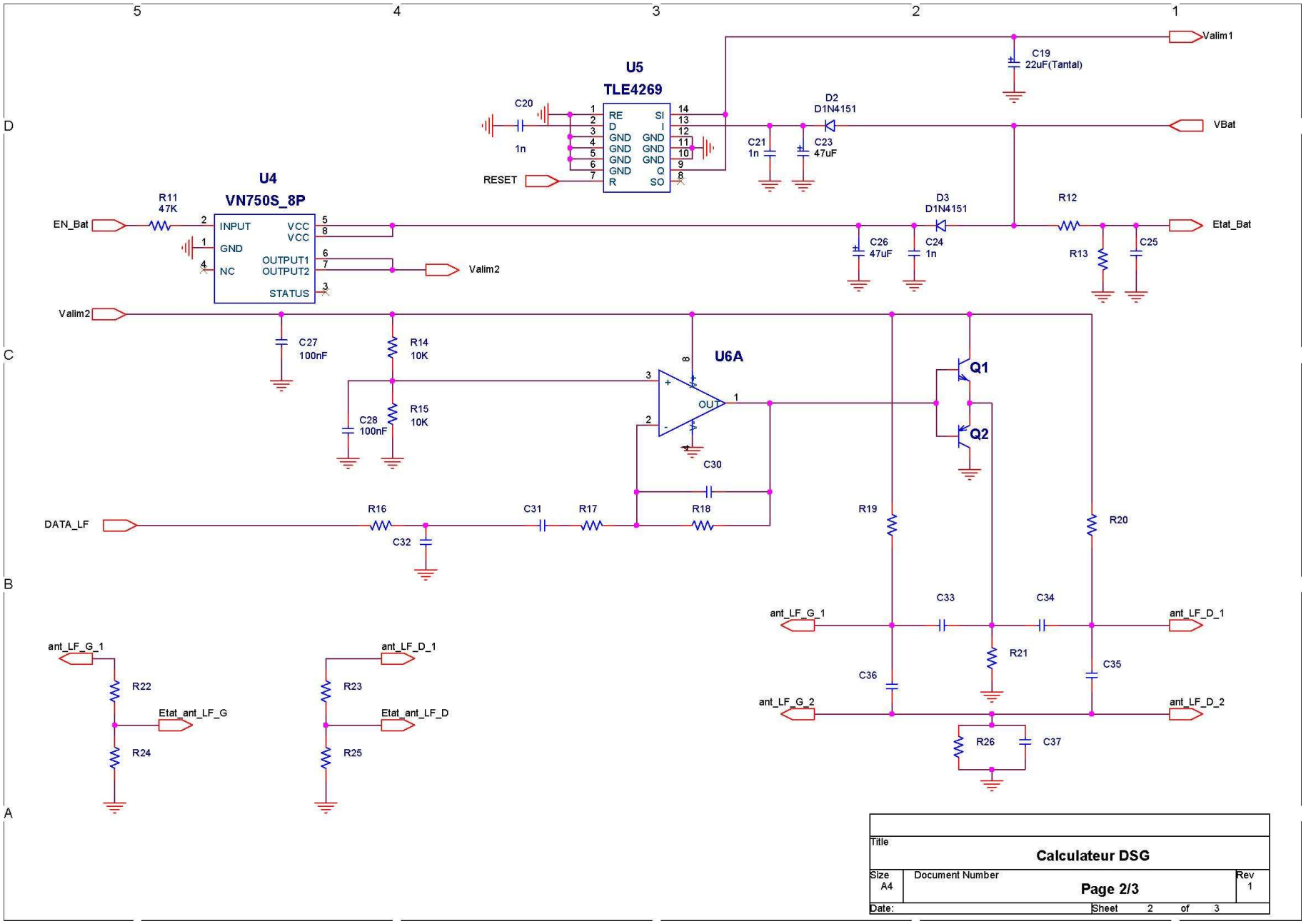
5
4
3
2
1
D
C
B
A
U5
TLE4269
C20
1n
RESET
RE
D
GND
GND
GND
GND
R
SI
I
GND
GND
Q
SO
C21
1n
D2
D1N4151
C23
47uF
C19
22uF(Tantal)
Valim1
VBat
U4
VN750S_8P
R11
47K
EN_Bat
INPUT
GND
NC
VCC
VCC
OUTPUT1
OUTPUT2
STATUS
Valim2
D3
D1N4151
R12
R13
C25
C26
47uF
C24
1n
Etat_Bat
Valim2
C27
100nF
R14
10K
R15
10K
C28
100nF
U6A
OUT
C30
Q1
Q2
DATA_LF
R16
C32
C31
R17
R18
R19
R20
ant_LF_G_1
C33
C34
ant_LF_D_1
R21
C35
C36
ant_LF_G_2
ant_LF_D_2
R26
C37
ant_LF_G_1
R22
Etat_ant_LF_G
R24
ant_LF_D_1
R23
Etat_ant_LF_D
R25
Title
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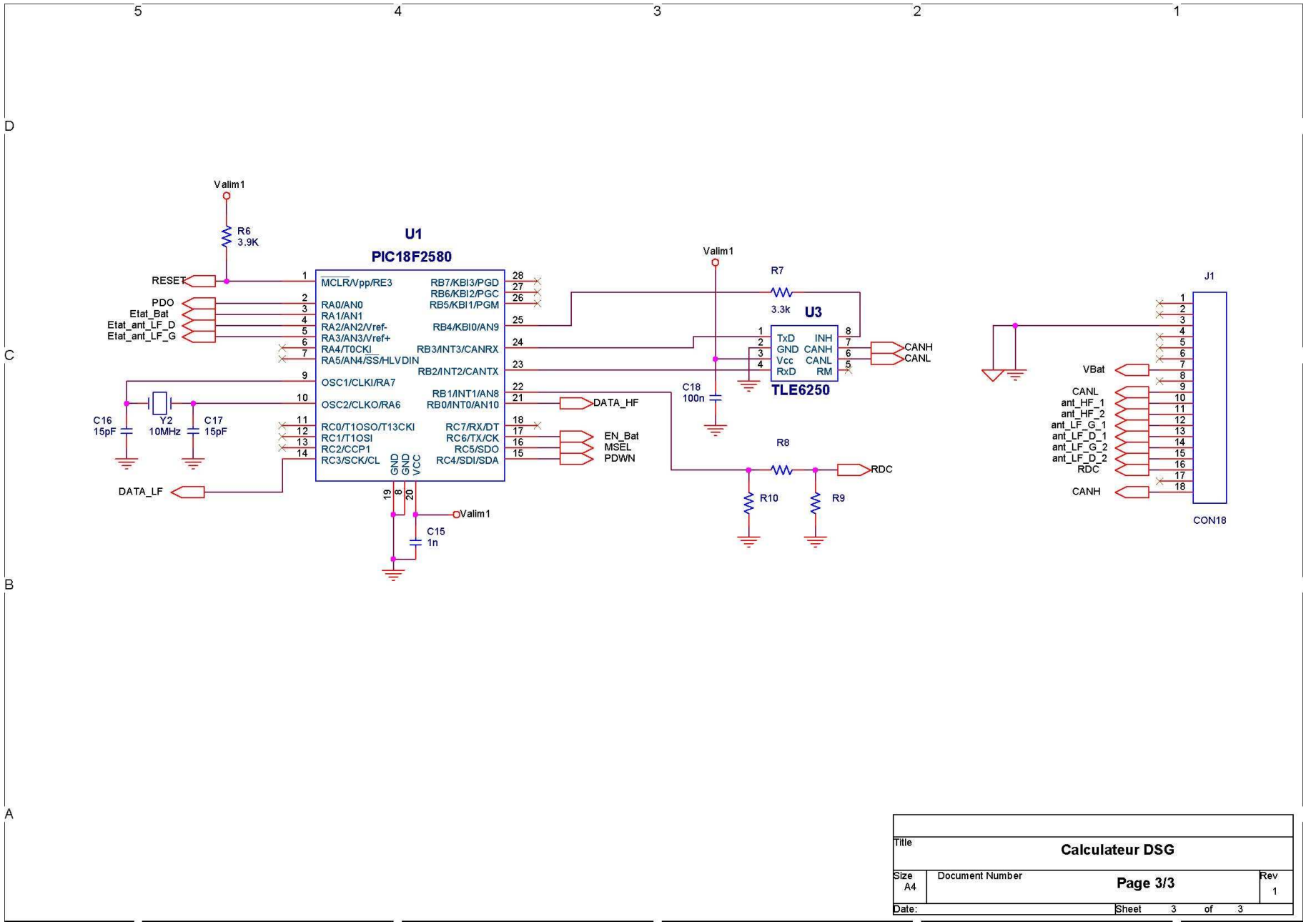
5
4
3
2
1
D
C
B
A
Valim1
R6
3.9K
U1
PIC18F2580
RESET
PDO
Etat_Bat
Etat_ant_LF_D
Etat_ant_LF_G
MCLR/Vpp/RE3
RA0/AN0
RA1/AN1
RA2/AN2/Vref-
RA3/AN3/Vref+
RA4/T0CKI
RA5/AN4/SS/HLVDIN
OSC1/CLKI/RA7
OSC2/CLKO/RA6
RC0/T1OSO/T13CKI
RC1/T1OSI
RC2/CCP1
RC3/SCK/CL
RB7/KBI3/PGD
RB6/KBI2/PGC
RB5/KBI1/PGM
RB4/KBI0/AN9
RB3/INT3/CANRX
RB2/INT2/CANTX
RB1/INT1/AN8
RB0/INT0/AN10
RC7/RX/DT
RC6/TX/CK
RC5/SDO
RC4/SDI/SDA
GND
GND
VCC
C16
15pF
Y2
10MHz
C17
15pF
DATA_LF
DATA_HF
EN_Bat
MSEL
PDWN
C15
1n
Valim1
R7
3.3k
U3
TLE6250
TxD
GND
Vcc
RxD
INH
CANH
CANL
RM
CANH
CANL
C18
100n
R8
RDC
R10
R9
J1
VBat
CANL
ant_HF_1
ant_HF_2
ant_LF_G_1
ant_LF_D_1
ant_LF_G_2
ant_LF_D_2
RDC
CANH
CON18
Title
Calculateur DSG
Size
A4
Document Number
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1
Date:
Sheet 3 of 3

Annexe: Bus CAN

Généralités

Le bus CAN (Controller Area Network) est né pour répondre au besoin d'assurer une communication de type série entre plusieurs calculateurs dans les véhicules automobiles. Ce bus a été développé par Bosch en 1983 et sa première normalisation référencée ISO11898 date de 1994. Depuis, la norme du protocole du bus CAN définit deux formats :

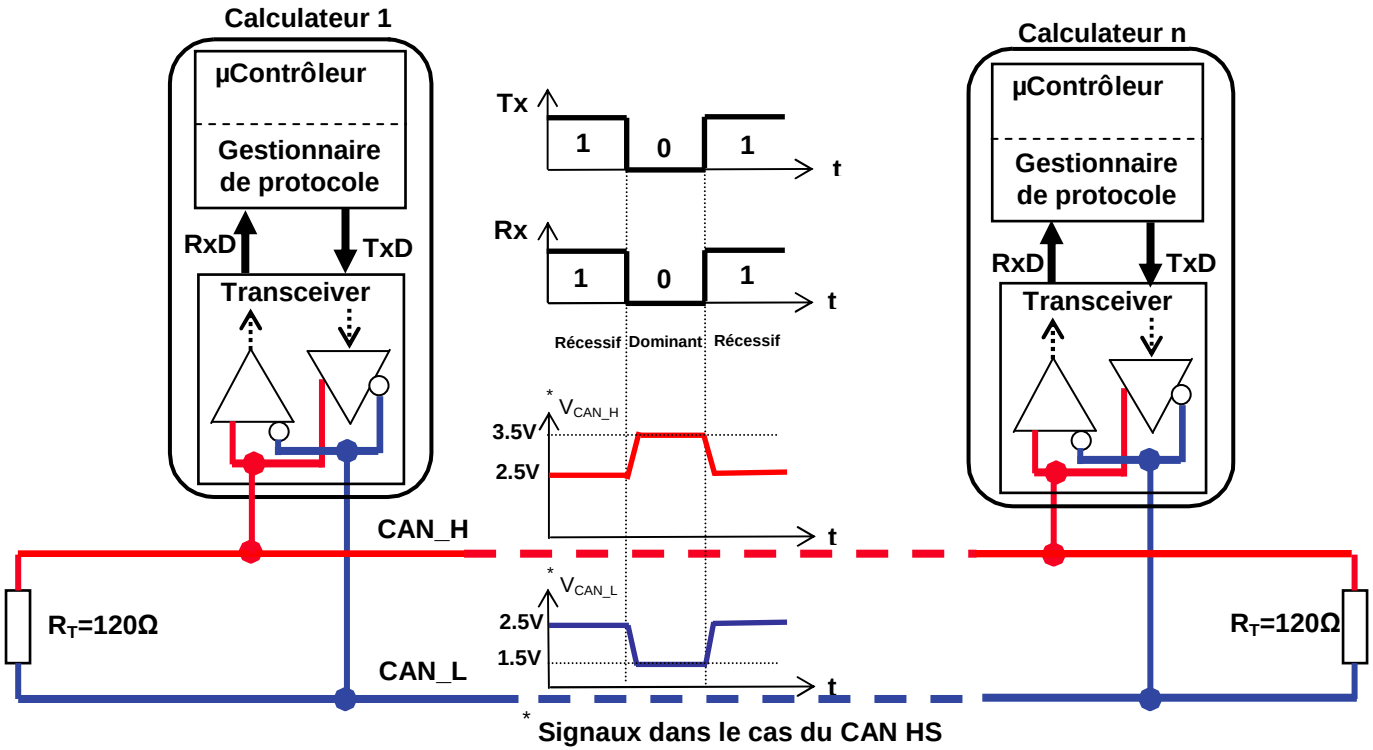
- Version **standard CAN 2.A** (champ identificateur sur **11 bits**)
- Version **étendu CAN 2.B** (champ identificateur sur **29 bits**)

La version du bus CAN utilisée dans cette épreuve est le CAN 2.A

Le débit de transmission sur le réseau CAN peut atteindre 1 Mbits/s. Deux classes de débits ont été également normalisées :

CAN Low Speed (noté **CAN LS**), dont le débit peut atteindre le **125 Kbits/s**.

CAN High Speed (noté **CAN HS**), de **125 kbits/s** jusqu'à **1 Mbits/s**.



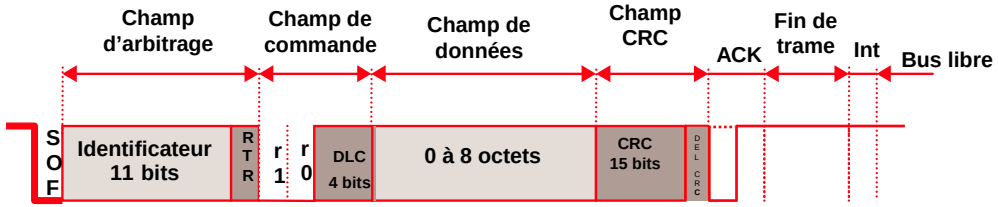
Comme illustré ci-dessus, un réseau CAN est constitué d'un medium (le support physique qui transporte le signal informationnel), qui souvent utilise deux fils électriques en différentiel : CAN_H et CAN_L. Cette paire de fils (généralement torsadée pour des problèmes de CEM) est raccordée à chaque calculateur (on dit souvent nœud) par une paire d'amplificateurs différentiels (un pour la transmission et l'autre pour la réception) intégrés dans un boîtier appelé transceiver (ou interface ligne).

Le nombre de calculateurs branchés sur la même paire est limité. La paire de fils est chargée par deux résistances de terminaison (R_T=120Ω chacune).

Le transceiver est relié au bloc gestionnaire du protocole CAN par deux lignes logiques : transmission (Tx) et réception (Rx).

Le gestionnaire du protocole CAN comporte des buffers d'émission, des buffers et des filtres de messages en réception. Souvent, le µcontrôleur intègre le gestionnaire du protocole CAN.

Format d'une trame standard CAN 2.A



SOF (Start of Frame)

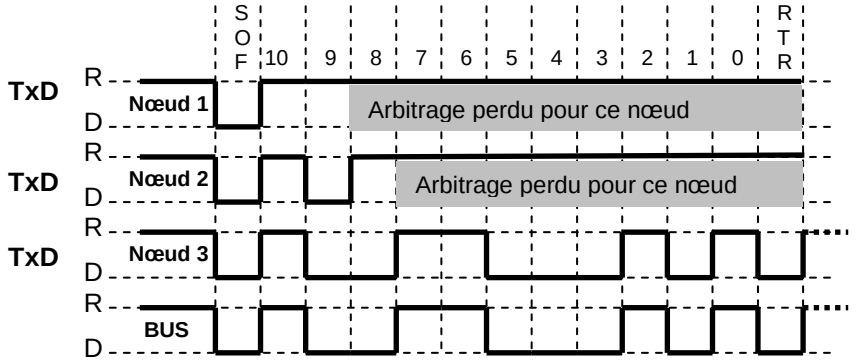
Constitué par un seul bit, de niveau dominant, indique aux nœuds le début de la trame. La détection du front descendant du **SOF** par les nœuds va leur permettre de se synchroniser sur la trame en cours de transmission.

Champ d'arbitrage

Constitué de l'identificateur du message (11 bits en trame standard) et du bit **RTR** (**R**emote **T**ransmission **R**equest). L'identificateur de longueur 11 bits permet d'attribuer une adresse spécifique à chaque message. Le bit de poids fort de l'identificateur est transmis en premier. Le bit **RTR** de niveau dominant indique que c'est une trame de données qui est en cours de transmission. Le bit **RTR** de niveau récessif indique que c'est une trame de requête (absence du champ de données) qui est en cours de transmission. La trame de requête est envoyée par un nœud à un autre nœud pour lui demander un renvoi de ses données.

Le champ d'arbitrage influe sur l'attribution du bus dans le cas où deux nœuds ou plus émettent simultanément leurs trames. Pour éviter les collisions et par conséquent la destruction de la trame, l'arbitrage du bus CAN s'appuie sur l'évaluation des identificateurs commençant la trame. Chaque nœuds débute son émission par l'identificateur composé de bits dominants et de bits récessifs. A travers son transceiver (on écoute ce que l'on émet : rebouclage du **TxD** sur le **RxD**), il compare chaque bit qu'il transmet sur le bus et le bit réellement transmis. En transmettant un bit récessif et après lecture du RxD, il détecte un bit dominant, le nœud s'aperçoit qu'il a perdu l'arbitrage. **Par conséquent, à partir du bit suivant, il se met en position récepteur**. Il tentera un accès au bus à la fin de transmission de la trame en cours.

Ci-dessous, une illustration du processus d'arbitrage entre 3 nœuds qui veulent accéder simultanément au bus :



R : Récessif

D : Dominant

Finalement, c'est le nœud 3 qui gagne le bus.

Champ de commande

Constitué de 6 bits :

2 bits **r1** et **r0** : sont réservés et toujours au niveau dominant.

4 bits formant le champ **DLC** qui indiquent le nombre d'octets qui seront transmis dans le champ de données.

Champ de données

Constitué de 0 à 8 octets maximums de données utiles, l'octet le plus significatif est transmis en premier et les bits de l'octet sont transmis dans l'ordre MSB.....LSB.

Champ CRC

C'est un code de contrôle, constitué de **15 bits,** suivi d'un **bit délimiteur** au **niveau récessif**.

Champ d'acquittement : ACK

Constitué de 2 bits : **ACK SLOT** suivi d'un **ACK délimiteur** qui est **récessif**. Quant au **ACK SLOT**, le nœud émetteur le met au niveau récessif (libération du bus pendant la durée d'un bit) et c'est un des nœuds récepteurs qui doit le mettre au niveau dominant pour acquitter la trame signifiant qu'elle a été bien reçue.

Fin de trame : EOF

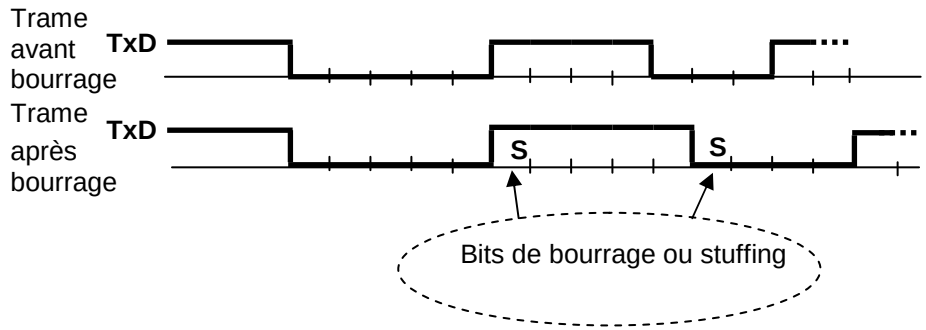
Constitué de **7 bits** au niveau **récessif**, il permet d'identifier la fin de la trame.

Technique de bit de bourrage « stuffing »

La synchronisation des nœuds récepteurs sur le nœud émetteur exploite les transitions entre les niveaux récessif et dominant. Pour éviter une longue suite de niveaux identiques, le gestionnaire du protocole introduit (au niveau de la transmission **TxD**), après 5 bits de niveaux identiques (dominant ou récessif), un bit supplémentaire de niveau opposé pour casser le rythme, c'est ce qu'on appelle le bit de « bourrage » ou de « stuffing ».

Cette technique allonge bien sûr la longueur de la trame et donc le temps de sa transmission. Quant aux nœuds récepteurs, ils feront l'opération inverse, c'est-à-dire, enlever les bits de « stuffing » (qui peuvent être présents dans le signal **RxD**) avant de traiter le contenu de la trame.

Voici un exemple qui illustre la technique de bourrage :



1 Product Description

1.1 Overview

The SP30 Tire Pressure Monitoring (TPM) Sensor represents Infineon's standard pressure range TPM sensor. The SP30 offers a high level of integration by including a microcontroller, signal conditioning and LF-input stage to meet market demands for flexible, customer specific solutions and overall system cost reduction.

The sensor design is based on Infineon's proprietary and patented solutions for high reliability measurements in harsh automotive environments. Its predictable and stable quality is proven in high volume applications.

The SP30 measures pressures up to 900kPa, temperature, supply voltage and acceleration (optional), and by integrating these functions with an ASIC in one package, Infineon has developed the ideal product for standard pressure TPM applications.

1.2 Features

- Integrated Sensors
  - Pressure
  - Acceleration (optional)
  - Temperature
  - Voltage
- Integrated Peripherals
  - Microcontroller
  - On board EEPROM
  - GPIOs
  - ADC for signal conditioning
  - 2x LF Receiver for triggering
- Measurement Ranges
  - Pressure Sensor 100 to 450 kPa / 100 to 900kPa
  - Temperature Sensor -40 to +125°C
  - Supply Voltage Sensor 2.1 to 3.6 V
  - Acceleration Sensor -12 to 115 g

2 Product Characteristics

The max and min values are to be understood as + and - 5σ values (Cpk = 1.67) unless otherwise specified.

2.1 Measurement performance

2.1.1 Pressure measurement

The presented performance reflects the use of 11-bit measurement of pressure signal and 10-bit measurement of temperature.

2.1.1.1 Standard pressure measurement range

Table 1 Pressure measurement specifications, 100-450kPa range

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	Temp [°C]	VDD [V]	
Pressure range	100		450	kPa	-40 to 125	2.1 to 3.6	
Measurement error	-7		7	kPa	0 to 50	2.1 to 3.6	
	-9		9	kPa	50 to 70	2.1 to 3.6	
	-17.5		17.5	kPa	-40 to 125	2.1 to 3.6	

2.1.1.2 Optional pressure measurement ranges

Table 2 Pressure measurement specifications, 100-700kPa range

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	Temp [°C]	VDD [V]	
Pressure range	100		700	kPa	-40 to 125	2.1 to 3.6	
Measurement error	-11		11	kPa	0 to 50	2.1 to 3.6	
	-14		14	kPa	50 to 70	2.1 to 3.6	
	-28		28	kPa	-40 to 125	2.1 to 3.6	

Table 3 Pressure measurement specifications, 100-800kPa range

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	Temp [°C]	VDD [V]	
Pressure range	100		800	kPa	-40 to 125	2.1 to 3.6	
Measurement error	-12.5		12.5	kPa	0 to 50	2.1 to 3.6	
	-16		16	kPa	50 to 70	2.1 to 3.6	
	-19.5		19.5	kPa	-40 to 125	2.1 to 3.6	

Table 4 Pressure measurement specifications, 100-900kPa range

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	Temp [°C]	VDD [V]	
Pressure range	100		900	kPa	-40 to 125	2.1 to 3.6	
Measurement error	-14		14	kPa	0 to 50	2.1 to 3.6	
	-18		18	kPa	50 to 70	2.1 to 3.6	
	-35		35	kPa	-40 to 125	2.1 to 3.6	

2.1.2 Acceleration measurement

The presented performance reflects the use of 12-bit measurement of acceleration signal and 10-bit measurement for temperature.

Table 5 Acceleration measurement specifications

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	Temp [°C]	VDD [V]	
Input range	-12		115	g	-40 to 90	2.1 to 3.6	
Sensitivity accuracy	-18.75		18.75	%	-40 to 90	2.1 to 3.6	
Offset accuracy	-6		6	g	-20 to 70	2.1 to 3.6	
	-8.5		8.5	g	-40 to 90	2.1 to 3.6	

2.1.3 Temperature measurement

The presented performance reflects the use of 10-bit measurement of temperature.

Table 6 Temperature measurement specifications

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	Temp [°C]	VDD [V]	
Measurement error	-3		3	°C	-20 to 70	2.1 to 3.6	
	-5		5	°C	-40 to 90	2.1 to 3.6	
	-3		7	°C	90 to 125	2.1 to 3.6	

2.1.4 Supply voltage measurement

The presented performance reflects the use of 9-bit measurement of supply voltage.

Table 7 Supply voltage measurement specifications

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	TEMP [°C]	VDD [V]	
Measurement error	-100		+100	mV	-40 to 125	V_{THR} to 3.6	

2.5 Clock sources

2.5.1 System clock (MCLK)

Table 11 System clock (MCLK) specifications

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	TEMP [°C]	VDD [V]	
MCLK frequency	1.8	2.0	2.2	MHz	-40 to 125	2.1 3.6	

2.5.2 Low Power (LP) oscillator

Table 12 LP oscillator specifications

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	TEMP [°C]	VDD [V]	
T_{it}	0.5, 1.0, 2.0 or 4.0			s	-40 to 125	2.1 to 3.6	Interval timer main tick
del_{2t}	25, 50, 75 or 100			ms	-40 to 125	2.1 to 3.6	Delay to extra tick
LP oscillator accuracy	-20		20	%	-40 to 125	2.1 to 3.6	

2.5.3 External clock

Table 13 External clock specifications

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	TEMP [°C]	VDD [V]	
External clock			3.5	MHz	-40 to 125	2.1 to 3.6	

2.6 LF input

Table 14 LF telegram

PARAMETER	SPECIFICATION				AMBIENT CONDITIONS		COMMENTS
	Min	Typ	Max	Unit	TEMP [°C]	VDD [V]	
Modulation		ASK			-40 to 125	2.1 to 3.6	
Carrier frequency	121.25	125	128.75	kHz	-40 to 125	2.1 to 3.6	
Preamble period	4			ms	-40 to 125	2.1 to 3.6	
Data rate	3.84	3.9	3.96	kHz	-40 to 125	2.1 to 3.6	
Settling time			2	ms	-40 to 125	2.1 to 3.6	Time from LF interface is turned on by RISC to the LF interface is active
Detection threshold			5	mVp-p	-40 to 125	2.1 to 3.6	
Input capacitance		10	12	pF	-40 to 125	2.1 to 3.6	
Input resistance	500			kΩ	-40 to 125	2.1 to 3.6	
Other	The input signals from the enabled LF channels are rectified and real time summed						

6 Pin Configuration

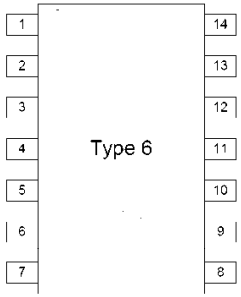
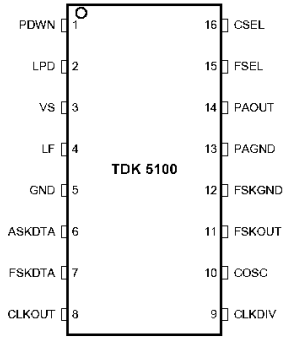


Figure 3: Pin Configuration. Top view, not to scale

Table 20 Pin Description

PIN	NAME	FUNCTION
1	IN4	LF receiver channel 2, negative input
2	P10	General purpose I/O with external wakeup, internal pull-up/pull-down
3	P11	General purpose I/O with external wakeup, internal pull-up/pull-down
4	MSDA	Monitor Serial Data I/O, internal pull-up
5	MSCL	Monitor Serial Clock input
6	VDD	Supply pad VDD (battery, positive terminal)
7	VSS	Common ground (battery, negative terminal)
8	VSS	Common ground (battery, negative terminal)
9	P17	General purpose I/O (or digital modulator output)
10	P15	General purpose I/O or external clock
11	P14	General purpose I/O (or digital modulator output)
12	IN1	LF receiver channel 1, positive input
13	IN2	LF receiver channel 1, negative input
14	IN3	LF receiver channel 2, positive input

2.1 Pin Configuration



Pin_config.wmf

Figure 2-1 IC Pin Configuration

Pin No.	Symbol	Function
1	PDWN	Power Down Mode Control
2	LPD	Low Power Detect Output
3	VS	Voltage Supply
4	LF	Loop Filter
5	GND	Ground
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	CLKOUT	Clock Driver Output
9	CLKDIV	Clock Divider Control (847.5 kHz or 3.34 MHz)
10	COSC	Crystal Oscillator Input
11	FSKOUT	Frequency Shift Keying Switch Output
12	FSKGND	Frequency Shift Keying Ground
13	PAGND	Power Amplifier Ground
14	PAOUT	Power Amplifier Output
15	FSEL	Frequency Range Selection (433 or 868 MHz)
16	CSEL	Crystal Frequency Selection (6.78 or 13.56 MHz)

2.3 Functional Block diagram

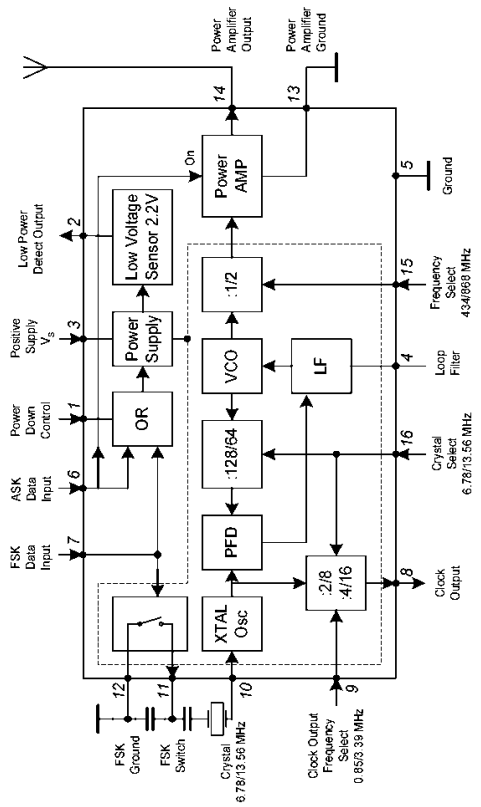


Figure 2-2 Functional Block diagram

2.4 Functional Blocks

2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 869 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 128 in case of a 6.78 MHz crystal or 64 in case of a 13.56 MHz crystal and can be selected via CSEL (pin 16). The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

2.4.2 Crystal Oscillator

The crystal oscillator operates either at 6.78 MHz or at 13.56 MHz.

The reference frequency can be chosen by the signal at CSEL (pin 16).

CSEL (pin 16)	Crystal Frequency
Low[1)]	6.78 MHz
Open[2)]	13.56 MHz

1) Low: Voltage at pin < 0.2 V
2) Open: Pin open

For both quartz frequency options, 847.5 kHz or 3.39 MHz are available as output frequencies of the clock output CLKOUT (pin 8) to drive the clock input of a micro controller.

The frequency at CLKOUT (pin 8) is controlled by the signal at CLKDIV (pin 9)

CLKDIV (pin 9)	CLKOUT Frequency
Low[1)]	3.39 MHz
Open[2)]	847.5 kHz

1) Low: Voltage at pin < 0.2 V
2) Open: Pin open

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 11).

The condition of the switch is controlled by the signal at FSKDTA (pin 7).

FSKDTA (pin7)	FSK Switch
Low[1]	CLOSED
Open[2], High[3]	OPEN

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

2.4.3 Power Amplifier

In case of operation in the 868-870 MHz band, the power amplifier is fed directly from the voltage controlled oscillator. In case of operation in the 433-435 MHz band, the VCO frequency is divided by 2. This is controlled by FSEL (pin 15) as described in the table below.

FSEL (pin 15)	Radiated Frequency Band
Low[1]	433 MHz
Open[2]	868 MHz

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open

The Power Amplifier can be switched on and off by the signal at ASKDTA (pin 6).

ASKDTA (pin 6)	Power Amplifier
Low[1]	OFF
Open[2], High[3]	ON

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

The Power Amplifier has an Open Collector output at PAOUT (pin 14) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 14) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 13) in order to reduce the amount of coupling to the other circuits.

TDK 5100

Functional Description

2.4.4 Low Power Detect

The supply voltage is sensed by a low power detector. When the supply voltage drops below 2.15 V, the output LPD (pin 2) switches to the low-state. To minimize the external component count, an internal pull-up current of 40 µA gives the output a high-state at supply voltages above 2.15 V.

The output LPD (pin 2) can either be connected to ASKDTA (pin 6) to switch off the PA as soon as the supply voltage drops below 2.15 V or it can be used to inform a micro-controller to stop the transmission after the current data packet.

2.4.5 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

2.4.5.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA at 3 V 25°C.

This current doubles every 8°C. The values for higher temperatures are typically 14 nA at 85°C and typically 600 nA at 125°C.

2.4.5.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 msec when the specified crystal is used.

The current consumption is typically 3.5 mA.

2.4.5.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

The current consumption of the IC is typically 7 mA when using a proper transforming network at PAOUT, see Figure 3-1.

2.4.5.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin 1). When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.
Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in Figure 3-5.

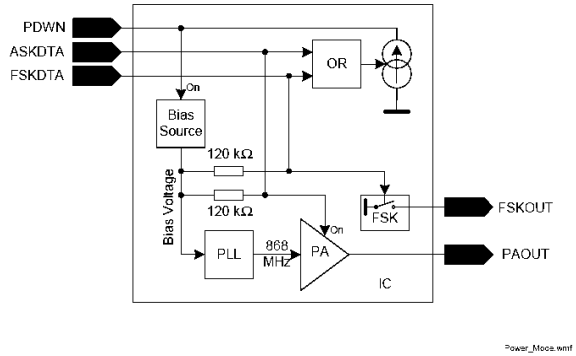


Figure 2-5 Power mode control circuitry

Table 3-8 provides a listing of how to get into the different power modes

PDWN	FSKDTA	ASKDTA	MODE
Low[1)]	Low, Open	Low, Open	POWER DOWN
Open[2)]	Low	Low	
High[3)]	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

1) Low: Voltage at pin < 0.7 V (PDWN)
Voltage at pin < 0.5 V (FSKDTA, ASKDTA)
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

2.4.6 Recommended timing diagrams for ASK- and FSK-Modulation

ASK Modulation using FSKDTA and ASKDTA, PDWN not connected

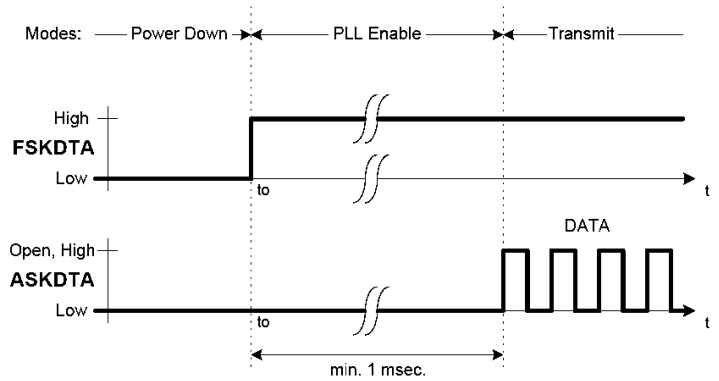


Figure 2-6 ASK Modulation

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected

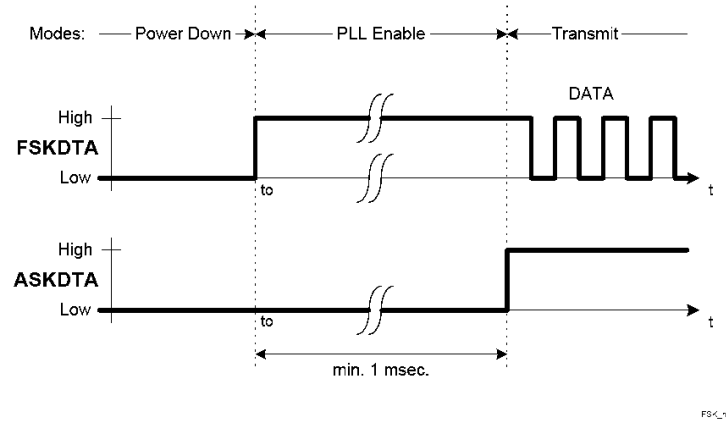


Figure 2-7 FSK Modulation

Alternative ASK Modulation, FSKDTA not connected.

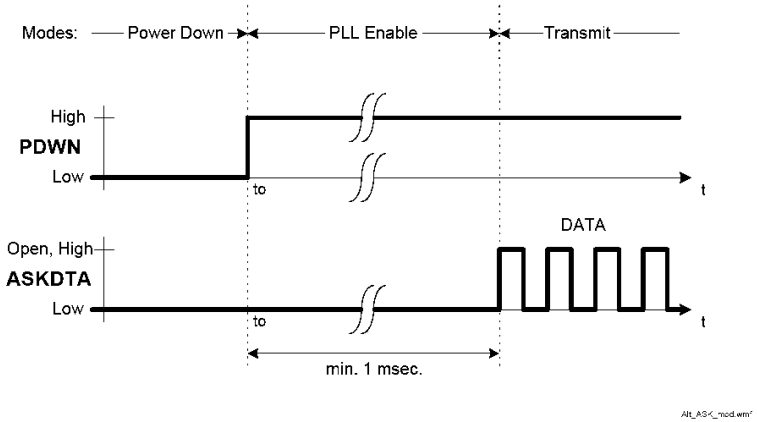


Figure 2-8 Alternative ASK Modulation

Alternative FSK Modulation

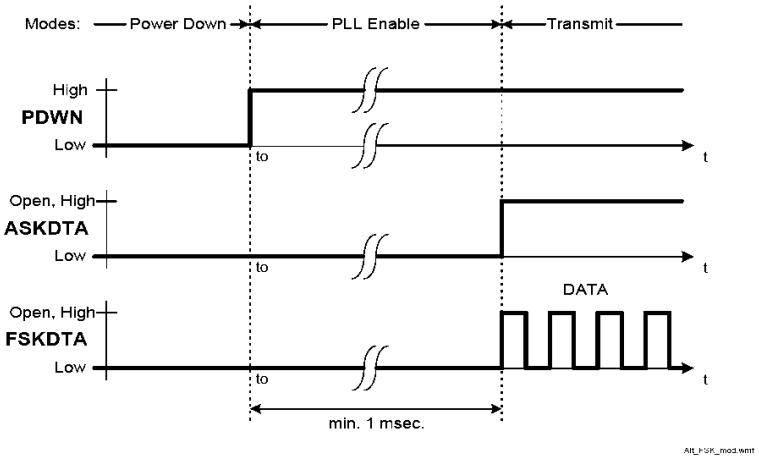


Figure 2-9 Alternative FSK Modulation

1 Product Description

1.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency bands 810 to 870 MHz and 400 to 440 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, an advanced data comparator (slicer) with selection between two threshold modes and a peak detector. Additionally there is a power down feature to save current and extend battery life, and two selectable alternatives of generating the data slicer threshold.

1.2 Features

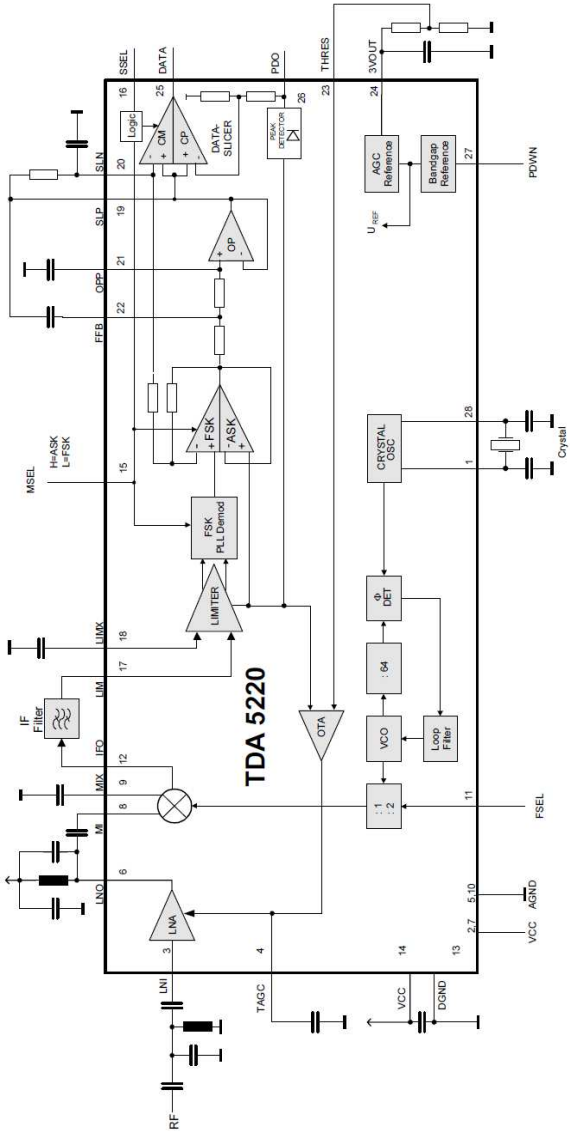
- Low supply current (Is = 5.7/5.9 mA typ. in FSK mode, Is = 5.0/5.2 mA typ. in ASK mode for 434/868 MHz)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity better than -106 dBm over specified temperature range (- 40 to +105°C)
- FSK sensitivity better than -100 dBm over specified temperature range (- 40 to +105°C)
- Selectable frequency ranges 810-870 MHz and 400-440 MHz
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with selection between two threshold modes (see **Section 2.4.8**)

1.3 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2-3 Fonctionnal Block Diagram

Figure 2



2.4 Functional Block Description

2.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 3.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 3.1.

2.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 400-440MHz/810-870MHz to the intermediate frequency (IF) at 10.7MHz with a vol-tage gain of approximately 21dB by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20MHz in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

2.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. The tuning range of the VCO guarantee over production spread and the specified temperature range is 820 and 860MHz. The oscillator signal is fed both to the synthesiser divider chain and to the downconverting mixer. In case of operation in the 400 to 440MHz range the signal is divided by two before it is fed to the Mixer. Depending on whether high- or low-side injection of the local oscillator is used, the receiving frequency ranges are 810 to 840MHz and 840 to 870MHz or 400 to 420MHz and 420 to 440MHz - see also Section 3.4. To be able to switch between two different frequency channels a divider ratio of either 32 or 32.25 can be selected via the FSEL-Pin.

Table 2 FSEL-Pin Operating States

FSEL	RF
Open	400-440MHz
GND	810-870MHz

2.4.4 Crystal Oscillator

The calculation of the value of the necessary crystal load capacitance is shown in Section 3.3, the crystal frequency calculation is explained in Section 3.4.

2.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be in its 'High'-state as described in the next chapter.

2.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 200µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with low frequencies applied to the demodulator demodulated to logic zero and high frequencies demodulated to logic ones. However this is only valid in case the local oscillator is low-side injected to the mixer which is applicable to receive frequencies above 840 or 420MHz. In case of receive frequencies below 840 or 420MHz high frequencies are demodulated as logical zeroes due to a sign inversion in the downconversion mixing process as the L0 is high-side injected to the mixer. See also Section 3.4.

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL** pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in Section 3.6.

Table 3 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

2.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order

Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 3.2.

2.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for subsequent circuits. A self-adjusting slicer-threshold on pin 20 its generated by a RC-term. In ASK-mode alternatively a scaled value of the voltage at the PDO-output (approx. 87%) can be used as the slicer-threshold as shown in Table 4. The data slicer threshold generation alternatives are described in more detail in Section 3.5.

Table 4 SSEL Pin Operating States

SSEL	MSEL	Selected Slicing Level (SL)
X	Low	external SL on Pin 20 (RC-term, e.g.)
High	High	external SL on Pin 20 (RC-term, e.g.)
Low	High	87% of PDO-output (approx.)

2.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. A capacitor is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. Note that the RSSI level is also output in case of FSK mode.

2.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 5 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On