DOCUMENTATION

Sommaire

Téléviseur LCD

Flat TV numérique 16/9
avec Digital Crystal Clear

32"

LCD Technologie numérique intégrée

Caractéristiques

Image/affichage

- Format d'image: 16/9
- Luminosité: 500 cd/m²
- Niveau de contraste (standard): 800:1
- Diagonale verrerie: 32 pouce
- Amélioration de l'image: Digital Crystal Clear, Contrast Plus, Progressive Scan, Filtre en peigne 3D, Compensation de mouvement 3/2 - 2/2, DNR (réduction numérique du bruit), Lissage des lignes obliques, Puce Pulse Killer, Active Control, Réglage de la température de couleur, Réglage de la netteté
- Amélioration de l'écran: Écran avec traitement antireflet
- Résolution d'écran: 1 366 x 768
- Temps de réponse (standard): 8 ms
- Angle de visualisation: 176° (H)/176° (V)
- Contraste écran dynamique: 1 600:1
- Type d'écran: Écran LCD WXGA à matrice active TFT

Résolution d'affichage prise en charge

- Formats informatiques

Résolution	Fréquence de rafraîchissement
640 x 480	60, 67, 72, 75 Hz
800 x 600	56, 60, 72, 75 Hz
1 024 x 768	60, 70, 75 Hz
720 x 400	70 Hz

- Formats vidéo

Résolution	Fréquence de rafraîchissement
640 x 480i	1Fh
640 x 480p	2Fh
720 x 576i	1Fh
720 x 576p	2Fh
1280 x 720p	3Fh
1920 x 1080i	2Fh

Son

- Accentuation du son: Amélioration dynamique des basses
- Système audio: Virtual Dolby Surround, Stéréo
- Puissance de sortie (RMS): 2 x 15 W
- Égaliseur: 5 bandes
- incrustation d'images: Picture in Graphics (PIG), Double écran télétexte
- Télécommande: DVD, Téléviseur, AUX
- Réglages du format d'écran: 4/3, Extension 14/9, Extension 16/9, Zoom sous-titrage, Super zoom, 16/9
- Horloge: Mise en veille programmable, Réveil
- Télétexte: Smart Text

Tuner/Réception/Transmission

- Bandes du tuner: Hyperband, S-Channel, UHF,
- système TV: PAL, SECAM
- Lecture vidéo: NTSC, PAL, SECAM
- Entrée antenne: Coaxiale 75 ohms (IEC75)
- Afficheur du tuner: PLL
- Nombre de présélections: 100
- DVB: DVB terrestre*

Connectivité

- Péritel Ext 1: Audio G/D, Entrée/sortie CVBS, RVB
- Péritel Ext 2: Entrée/sortie CVBS, Entrée S-Vidéo, Audio G/D, Sortie RVB
- Autres connexions: Interface commune, Sortie S/PDIF (coaxiale), Antenne IEC75
- Connexions avant/latérales: Entrée CVBS, Sortie casque, Entrée S-Vidéo, Entrée audio G/D
- Ext 4: YUV
- Ext 5: HDMI
- Ext 6: HDMI
- Nombre de péritel: 2

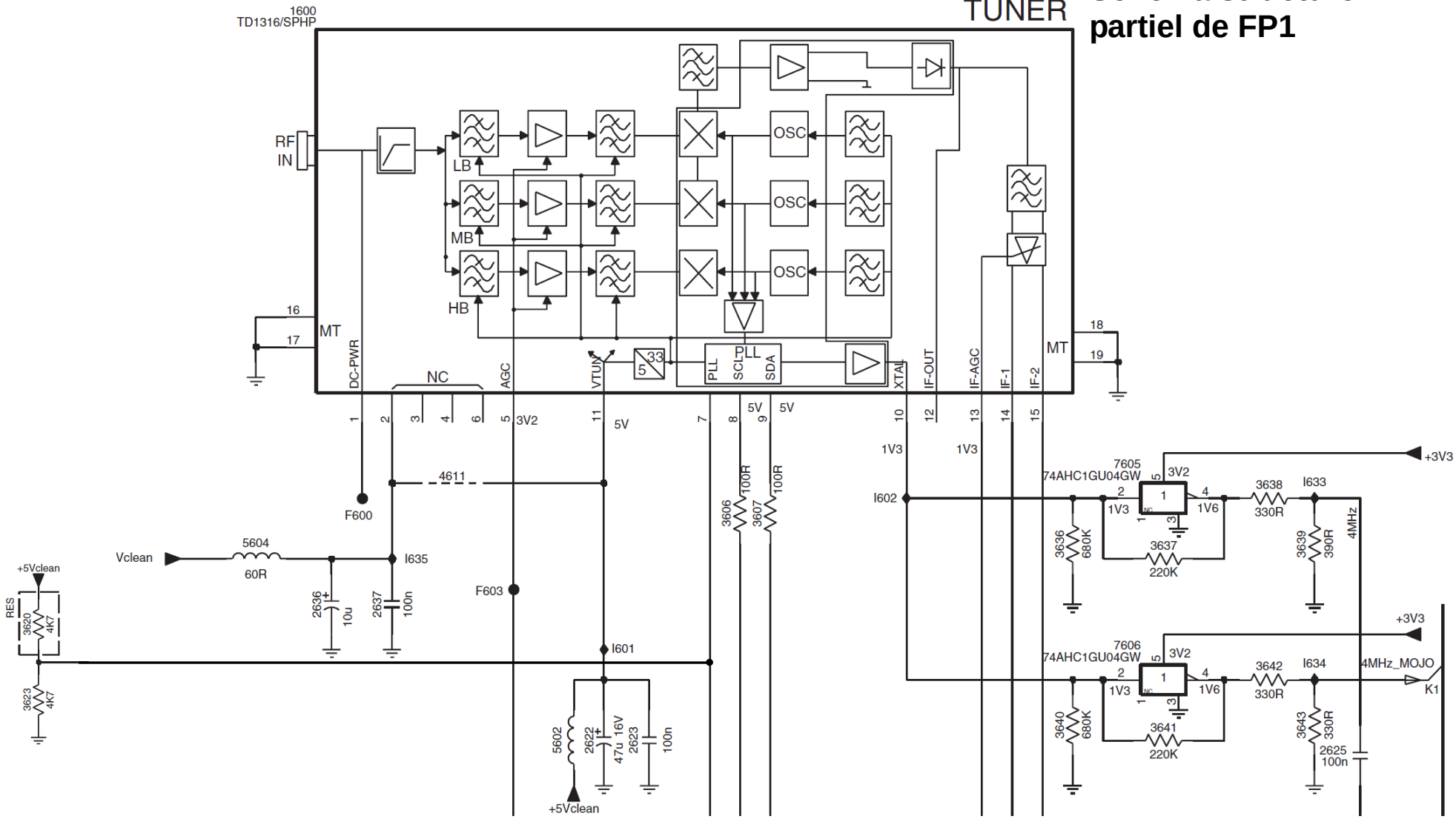
Alimentation

- Consommation: 125 W
- Consommation en veille: < 1 W
- Température ambiante: +5 -/+ 40 °C
- Secteur: 220 - 240 V CA +/- 10 %
- Alimentation: 90 - 240 V CA

Dimensions

- Poids de l'appareil: 18 9 kg
- Poids (emballage compris): 22 kg
- Dimensions (avec la base) (H x P): 550 x 222 mm

Schéma structurel partiel de FP1



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Tuner TDA 1316L

Tuner module for digital terrestrial (OFDM) applications — **TD(M)1300AL**

PRODUCT DESCRIPTION

TDM1300AL are tuners out of the new generation of high performance devices designed to cope with the digital terrestrial COFDM transmission standard.

The RF-downstream section is equipped with a state-of-the-art, 3-band, single conversion tuner which makes use of a highly integrated mixer-oscillator-PLL tuner-IC that provides the required high level of performance which becomes necessary for COFDM signal downstream.

FEATURES

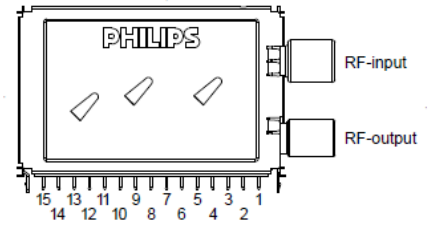
- Highly integrated RF-module, UHF modulator plus active loopthrough plus 3-band tuner
- +5V supply voltage only; no external tuning voltage required
- Tuners for horizontal and vertical mounting available
- Option with DC – power output through input connector (e.g. indoor antenna supply)
- Tuners comply with relevant CENELEC standards with regard to requirements concerning signal handling capability and immunity
- Superior low noise and high sensitivity performance

- RF-in to RF-out loopthrough amplifiers
  - Low noise and excellent linearity
  - Full VHF to UHF frequency range coverage
  - Standard connectors for in- and output e.g. IEC, F-connector, RCA

- High performance and cost effective single conversion tuner
  - I^2C programmable
  - 400kHz Bus compliant
  - Fast PLL tuning speed (programmable step size e.g. 62.5kHz and 166.67kHz)
  - Tuner internal gain control loop with selectable TakeOverPoint settings via I^2C Bus
    - External gain control possible with internal loop disabled
      - 4.0V (max. gain) to 0V (min. gain) gain control voltage
  - Flat overall frequency response
  - High PLL loop bandwidth which ensures very low oscillator phase noise
  - 4 MHz crystal reference frequency output
  - SAW-filter and IF-amplifier included
    - Switchable 7/8 MHz SAW filter (full band tuners)
    - Fixed 8 MHZ SAW filter (UHF only tuners)
    - IF-amplification controllable over a wide range

- Differential, filtered (SAW) 'digital' IF-output to directly drive the channel decoder

DEFINITION OF TERMINALS / SUPPLY DATA



Terminal	Function	Remark
1	DC-power option for tuners with P-extension	Max. permissible current: 100mA
	Option: DC-connection to TV-output terminal *(only for TDM1344L/IH, TDM1344L/IV, TD1344L/IV)*	Special version on customer request
2	+5V ± 5% splitter / modulator supply voltage	max. current = 127mA *(for tuners w. remodulator)* max. current = 40mA *(for tuners w/o remodulator)*
3	Audio - baseband input *(not connected for tuners w/o remodulator)*	AC - coupled
4	Video - baseband input *(not connected for tuners w/o remodulator)*	AC - coupled
5	External RF-gain control voltage (0.5V - 4.0V)	Max. permissible control voltage source impedance limited to 200ohms (see application notes)
6	do not connect, leave terminal open	for testing only
7	PLL chip address select (I^2C / tuner)	see application notes
8	SCL (I^2C / tuner)	
9	SDA (I^2C / tuner)	
10	4MHz reference frequency output;	AC coupled
11	+5V ± 5% supply tuner (V_{TU})	max. current = 170mA
12	'broadband' IF - output	AC coupled
13	IF-gain control voltage	max. gain at 3V min. gain at 0V (see application notes)
14	'narrowband' IF - output	AC coupled
15	'narrowband' IF - output	AC coupled

SPECIFICATION DATA

Next specification data refer to the overall performance from RF-input to IF-output.
If not otherwise stated, all data are assigned to broadband IF-output.
The tuner has to be tuned as such that coincidence between RF-channel center and IF-center frequency of 36.13MHz is given.

	MIN.	TYP.	MAX.
Frequency ranges (VHF/UHF) (1) *(VHF low) low-band* *(VHF high) mid-band* *(UHF) high-band* *UHF only tuners*	 49MHz 162MHz 448MHz 474MHz		 159MHz 444MHz 861MHz 861MHz
RF power gain (2)	47dB	50dB	
Overall gain taper		6dB	
RF AGC range *Low band* *Mid band* *High band*	 40dB 40dB 35dB		
Image rejection *(referred to IF-center frequency)* *(VHF low) low-band* *(VHF high) mid-band* *(UHF) high-band*	 66dB 66dB 55dB	 70dB 70dB 60dB	
Osc. voltage at aerial input (f < 1000MHz)		<20dBµV	
RF-input return loss (75ohms)	5dB	>7dB	
In-channel return loss (3)		8dB	
Overloading causing *1dB gain compression*		76dBµV	
Noise figure (at nom. gain)		5dB	7dB
ESD protection of terminals	2kV		
Surge protection at RF-input	5kV		
Osc. phase noise (4) *(1kHz)* *(10kHz)*		 -88dBc/Hz -90dBc/Hz	 -78dBc/Hz -82dBc/Hz
Overall voltage gain (5)		77dB	

Note 1: channel center including tuning margin
Note 2: to be measured at 'broadband' IF-output with 75ohms load
Note 3: to be measured at RF-input in the range channel-center ± 3MHz
Note 4: PLL step size 166.667kHz; CP as recommended (see application notes)
Note 5: measured at terminals 14/15; IF-AGC voltage (terminal 13) set to 3V

Frequency allocation table:

	TDM1316AL / TD1316AL	TDM1344L / TD1344L
RF frequency range	51MHz – 858MHz (*)	474MHz – 858MHz (*)
Channel bandwidth	7/8MHz	8 MHz
RF-loopthrough range	ch E2 - ch E69	ch E2 - ch E69
Modulator range (for tuners with modulator only)	ch E21 - ch E69	ch E21 - ch E69
IF-center frequency	36.13MHz	36.13MHz
RF input connector RF output connector	IEC female IEC male	IEC female IEC male

(*) data refer to RF-channel center frequency.

APPLICATION NOTES

Programming of tuner PLL

The tuner control (frequency selection and band switching) is done via the I^2C bus.
One address byte and four data bytes are needed to fully program the tuner.
A PLL lock flag can be read from the tuner during 'READ' - mode.
Four independent PLL addresses are available; which one is actually valid depends on the address select voltage that is connected to terminal 7.
TD(M)1316AL tuners comply to the 5V I^2C – Bus specification.

I^2C-bus data format , ' WRITE ' - mode:

NAME	BYTE	MSB							LSB	ACK
Addressbyte	1	1	1	0	0	0	CA1	CA0	R/W=0	A
Prog. Divider Byte 1	2	0	N14	N13	N12	N11	N10	N9	N8	A
Prog. Divider Byte 2	3	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Data Byte 1	4	1	D/A =1	0	0	1	R2	R1	R0	A
	4	1	D/A = 0	0	0	ATC	AL2	AL1	AL0	
Control Data Byte 2	5	CP2	CP1	CP0	SP5	SP4	SP3	SP2	SP1	A

A = acknowledge

Description of used symbols:

CA1, CA0 : chip address selection bits (see table: Programmable address selection bits)
R/W : Read / Write bit ; Bit = 0 ⇒ Write mode
Bit = 1 ⇒ Read mode
N14 to N0 : LO frequency divider bits
D/A : D/A = 1 ⇒ following 6 bits contain test and reference divider ratio data
: D/A = 0 ⇒ following 6 bits contain AGC setting data
R2, R1, R0 : reference divider bits (see table: Reference Divider Settings)
ATC : AGC time constant data bit; only valid with int. AGC loop active
ATC = 1 ⇒ enables fast tuning speed during channel search mode
ATC = 0 ⇒ recommended after channel acquisition; normal mode
AL2, AL1, AL0 : AGC Take-Over-Point bits (see table: Internal AGC loop TOP)
CP2, CP1, CP0 : PLL charge pump current selection bits (see table: Charge Pump Settings)
SP5 ..... SP1 : Switch ports; bit = 1 ⇒ port V_{out} is 'ON'
bit = 0 ⇒ port V_{out} is 'OFF'
(see table: Band and SAW-filter selection table)

CA1, CA0: Programmable address selection bits

CA1	CA0	*Voltage applied to terminal 7*
0	0	0V to $0.1xV_{TU}$
0	1	terminal open
1	0	$0.4xV_{TU}$ to $0.6xV_{TU}$
1	1	$0.9xV_{TU}$ to $1.0xV_{TU}$

N14 to N0: programmable divider bits

divider ratio: $N = N14x2^{14} + N13x2^{13} + ... + N1x2^{1} + N0$

How to calculate the divider ratio N :

$$N = \frac{(f_{input} + f_{IF})}{f_{ref}} \left[\frac{Hz}{Hz}\right] \quad \text{whereby} \quad f_{ref} = \frac{4 \cdot 10^6}{64^{(1)}}[Hz] = 62.5kHz$$

$$f_{ref} = \frac{4 \cdot 10^6}{24^{(1)}}[Hz] = 166.6\overline{7}kHz$$

Note (1) : divider ratio to be set with Bits ' R2 ..... R0 ' (see table below)

R2, R1, R0 : PLL reference divider settings (Control Data Byte 1):

PLL step size	PLL ref. divider ratio	R2	R1	R0
50.0 kHz	80	0	1	1
62.5 kHz	64	0	0	0
166.67 kHz	24	0	1	0

CP2, CP1, CP0: PLL charge pump current settings

Note: during search tuning it is recommended to set the PLL to a moderate charge pump. To enable best oscillator phase noise performance during digital signal processing, the PLL charge pump current should be set to conditions as given with following table.

In analog applications the PLL charge pump current must be set to max. 60uA !

CP2	CP1	CP0	Typical CP current	Recommendations
0	0	0	40 uA	
0	0	1	60 uA	
0	1	0	90 uA	**To be used during search tuning and for 50kHZ, 62.5kHz PLL step sizes**
0	1	1	130 uA	Low - band: 87MHz - 130MHz Mid - band: 200MHz - 290MHz High - band: 480MHz - 620MHz (*)
1	0	0	190 uA	
1	0	1	280 uA	Low - band: 130MHz - 160MHz Mid - band: 290MHz - 420MHz High - band: 620MHz - 830MHz (*)
1	1	0	410 uA	Low - band: >160MHz Mid - band: >420MHz (*)
1	1	1	600 uA	High - band: >830MHz (*)

(*) oscillator frequencies

SP5 ..... SP1: Band and SAW-filter selection table

	SP5	SP4	SP3	SP2	SP1
Low - band	0	X	0	0	1
mid - band	0	X	0	1	0
High - band	0	X	1	0	0

	SP5	SP4	SP3	SP2	SP1
7 MHz SAW - filter	0	0	X	X	X
8 MHz SAW - filter	0	1	X	X	X

Librairie delays

The delay functions execute code for a specific number of processor instruction cycles. For time based delays, the processor operating frequency must be taken into account. The following routines are provided:

TABLE 4-4: DELAY FUNCTIONS

Function	Description
`Delay1TCY`	Delay one instruction cycle.
`Delay10TCYx`	Delay in multiples of 10 instruction cycles.
`Delay100TCYx`	Delay in multiples of 100 instruction cycles.
`Delay1KTCYx`	Delay in multiples of 1,000 instruction cycles.
`Delay10KTCYx`	Delay in multiples of 10,000 instruction cycles.

4.5.1 Function Descriptions

Delay1TCY

Function: Delay 1 instruction cycle (TCY).

Include: `delays.h`

Prototype: `void Delay1TCY( void );`

Remarks: This function is actually a `#define` for the `NOP` instruction. When encountered in the source code, the compiler simply inserts a `NOP`.

File Name: `#define in delays.h`

Delay10TCYx

Function: Delay in multiples of 10 instruction cycles (TCY).

Include: `delays.h`

Prototype: `void Delay10TCYx( unsigned char unit );`

Arguments: ***unit***
The value of ***unit*** can be any 8-bit value. A value in the range [1,255] will delay (***unit*** * 10) cycles. A value of 0 causes a delay of 2,560 cycles.

Remarks: This function creates a delay in multiples of 10 instruction cycles.

Delay100TCYx

Function: Delay in multiples of 100 instruction cycles (TCY).

Include: `delays.h`

Prototype: `void Delay100TCYx( unsigned char unit );`

Arguments: ***unit***
The value of ***unit*** can be any 8-bit value. A value in the range [1,255] will delay (***unit*** * 100) cycles. A value of 0 causes a delay of 25,600 cycles.

Delay1KTCYx

Function: Delay in multiples of 1,000 instruction cycles (TCY).

Include: `delays.h`

Prototype: `void Delay1KTCYx( unsigned char unit );`

Arguments: ***unit***
The value of ***unit*** can be any 8-bit value. A value in the range [1,255] will delay (***unit*** * 1000) cycles. A value of 0 causes a delay of 256,000 cycles.

Delay10KTCYx

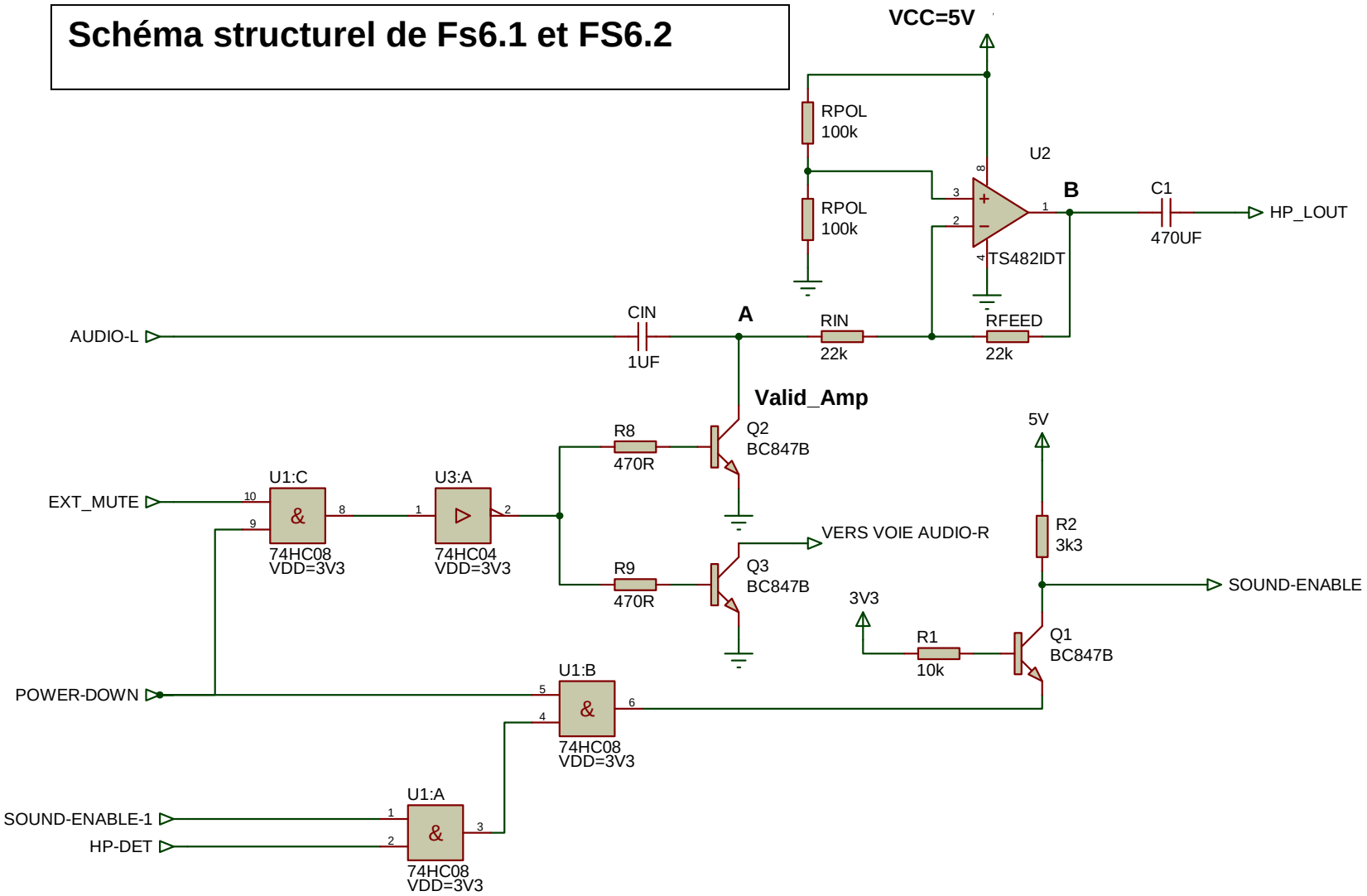
Function: Delay in multiples of 10,000 instruction cycles (TCY).

Include: `delays.h`

Prototype: `void Delay10KTCYx( unsigned char unit );`

Arguments: ***unit***
The value of ***unit*** can be any 8-bit value. A value in the range [1,255] will delay (***unit*** * 10000) cycles. A value of 0 causes a delay of 2,560,000 cycles.

Schéma structurel de Fs6.1 et FS6.2



- Operating from **Vcc=2V to 5.5V**
- 100mW into 16Ω at 5V
- 38mW into 16Ω at 3.3V
- 11.5mW into 16Ω at 2V
- Switch ON/OFF click reduction circuitry
- High power supply rejection ratio: 85dB at 5V
- High signal-to-noise ratio: 110dB(A) at 5V
- High crosstalk immunity: 100dB (F=1kHz)
- Rail-to-rail input and output
- Unity-gain stable

Applications

- Stereo headphone amplifier
- Optical storage
- Computer motherboard
- PDA, organizers & notebook computers
- High-end TV, set-top box, DVD players
- Sound cards

TS482

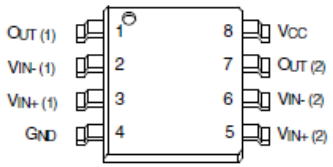
Description

The TS482 is a dual audio power amplifier able to drive a 16 or 32Ω stereo headset down to low voltages.

It is delivering up to 100mW per channel (into 16Ω loads) of continuous average power with 0.1% THD+N from a 5V power supply.

The unity gain stable TS482 can be configured by external gain-setting resistors.

TS482ID, TS482IDT - SO-8



Typical application schematic

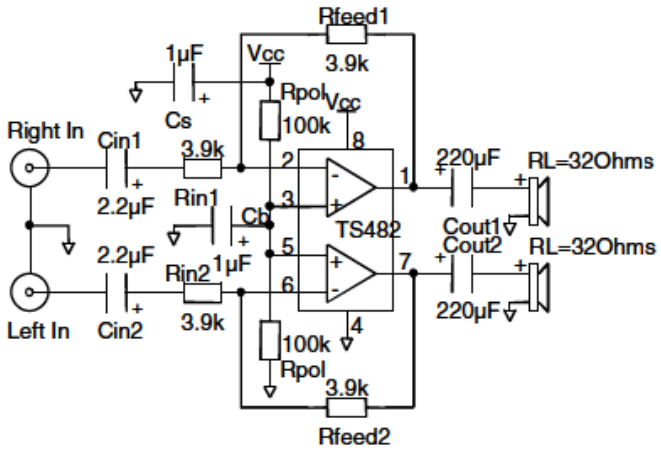
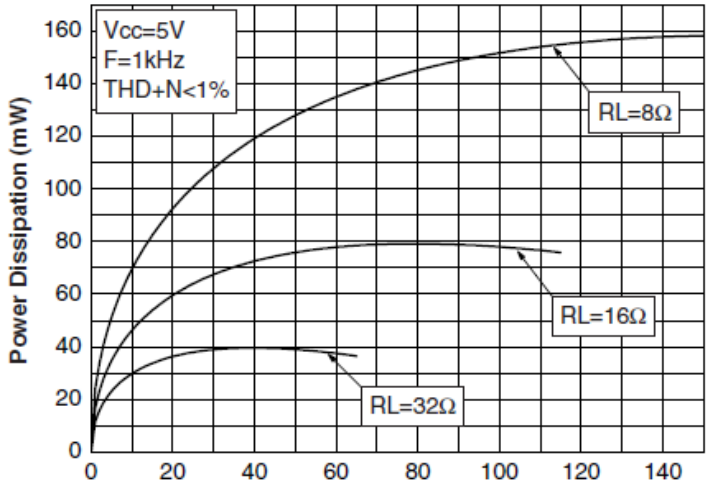
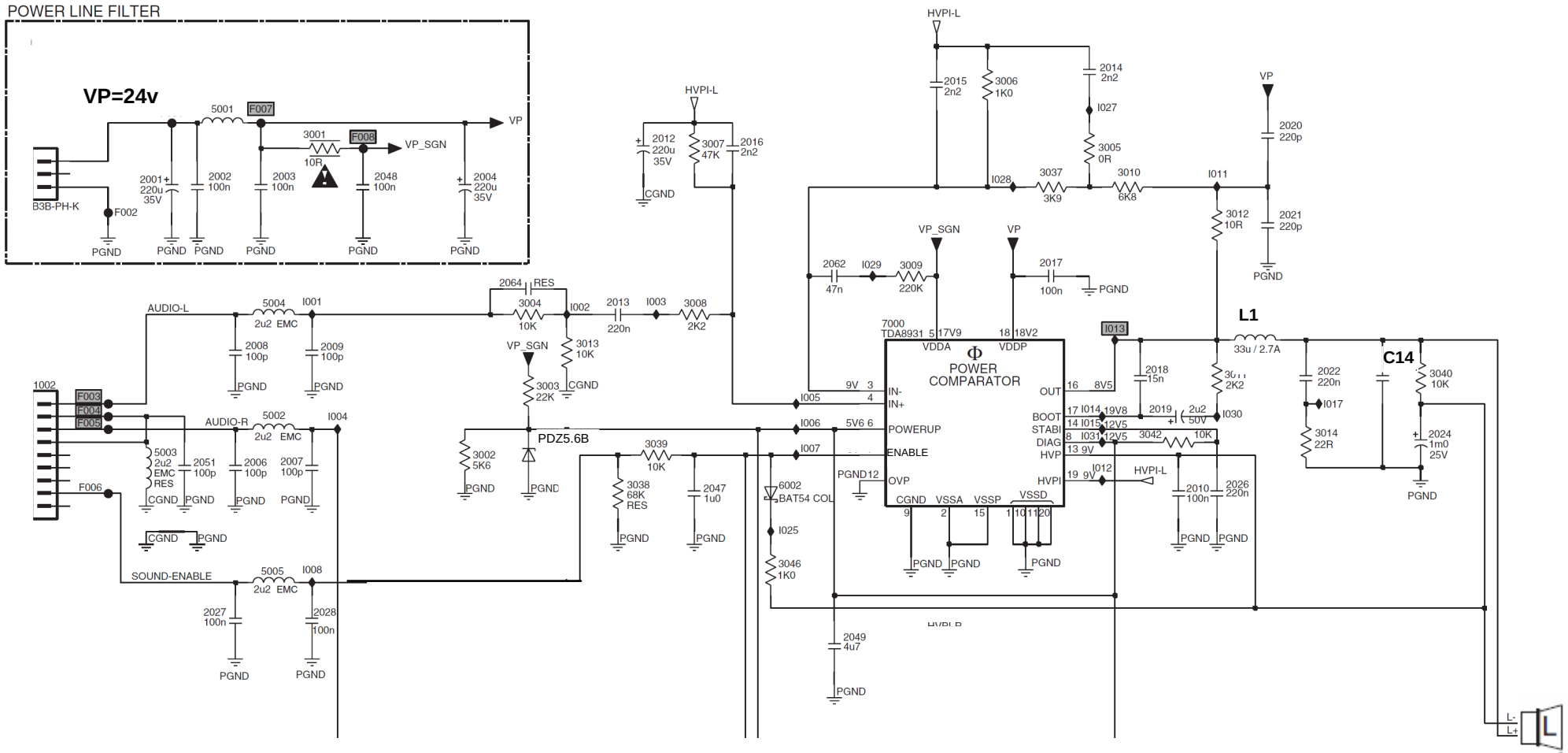


Table 7. Components description

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin (fc = 1 / (2 x Pi x Rin x Cin))
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply Bypass capacitor which provides power supply filtering
Cb	Bypass capacitor which provides half supply filtering
Cout	Output coupling capacitor which blocks the DC voltage at the load input terminal This capacitor also forms a high pass filter with RL (fc = 1 / (2 x Pi x RL x Cout))
Rpol	These 2 resistors form a voltage divider which provide a DC biasing voltage (Vcc/2) for the 2 amplifiers.
Av	Closed loop gain = -Rfeed / Rin

Figure 28. Power dissipation vs. output power





Vers voie droite

Schéma structurel de FS6.3
Amplification classe D

TDA8931

Power comparator 1 × 20 W

Rev. 01 — 14 January 2004 Preliminary data sheet

1. General description

The TDA8931 is a switching power stage for high efficiency class-D audio power amplifier systems.

It contains a Single-Ended (SE) power stage, drive logic, protection control logic, a full differential input comparator and a HVP charger to charge the SE capacitor. With this amplifier a compact 1 × 20 W closed loop self-oscillating digital amplifier system can be built. The TDA8931 has a high efficiency so that a heat sink is not required up to 20 W (RMS). The system operates on an asymmetrical and a symmetrical supply voltage.

7. Pinning information

7.1 Pinning

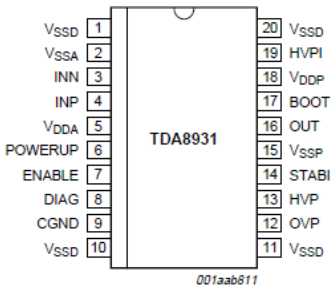


Fig 2. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
V_{SSD}	1	negative digital supply voltage; heat spreader
V_{SSA}	2	negative analog supply voltage
INN	3	inverting input
INP	4	non inverting input
V_{DDA}	5	positive analog supply voltage
POWERUP	6	power-up input
ENABLE	7	enable input
DIAG	8	diagnostic output
CGND	9	control ground; reference ground for pins POWERUP, ENABLE and DIAG
V_{SSD}	10	negative digital supply voltage; heat spreader
V_{SSD}	11	negative digital supply voltage; heat spreader
OVP	12	overvoltage protection reference input
HVP	13	half supply voltage output for charging SE capacitor
STABI	14	decoupling of internal stabilizer
V_{SSP}	15	negative power supply voltage
OUT	16	PWM output
BOOT	17	bootstrap capacitor connection
V_{DDP}	18	positive power supply voltage
HVPI	19	half supply voltage output for reference voltage of input circuitry
V_{SSD}	20	negative digital supply voltage; heat spreader

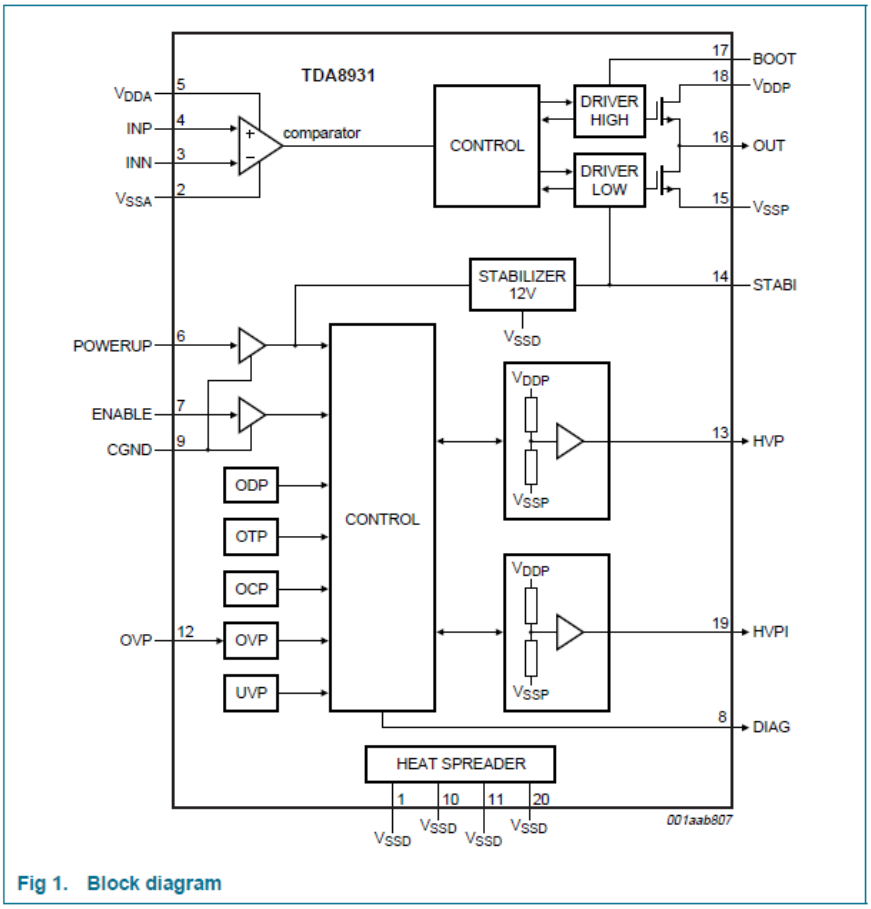


Fig 1. Block diagram

8. Functional description

8.1 General

The TDA8931 is a switching power stage for high efficiency class-D audio power amplifier systems. It contains a Single-Ended (SE) power stage, drive logic, protection control logic, a full differential input comparator and a HVP charger to charge the SE capacitor (see Figure 1). With this amplifier a compact 1 × 20 W closed loop self-oscillating digital amplifier system can be built. A second order low-pass filter converts the PWM output signal into an analog audio signal across the speaker.

8.2 Interfacing

The operating modes of the TDA8931 can be controlled by pins POWERUP and ENABLE. Both pins refer to pin CGND. The device has three modes:

- Sleep mode
- Standby mode
- Operating mode

When pin POWERUP = LOW, the power comparator is in Sleep mode, independent of the signal on pin ENABLE. In Sleep mode the SE capacitor charger will be discharged.

When pin POWERUP = HIGH and pin ENABLE = LOW the device is in Standby mode. In Standby mode the device is DC biased and the SE capacitor will be charged and the output is floating.

When both pins POWERUP and ENABLE are HIGH, the device is in Operating mode. A level at pin POWERUP greater than 11 V can also enter the Operating mode, independent of the level on pin ENABLE (see Table 4).

Remark: The switch-on sequence is important. First pin POWERUP = HIGH, then pin ENABLE = HIGH.

Table 4: Interfacing

Voltage on pin		Mode
POWERUP	ENABLE	
< 0.8 V	-	Sleep
3 V to 7 V	< 0.8 V	Standby
	> 3 V	Operating
> 11 V	-	Operating

10. Limiting values

Table 7: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	operating supply voltage	asymmetrical	12	40	V
		symmetrical	±6	±20	V
V_{ENABLE}	maximum voltage on pin ENABLE		-	14	V
V_{OVP}	maximum voltage on pin OVP		-	14	V
V_n	voltage on all other pins		V_{SS} – 0.3	V_{DD} + 0.3	V
I_{ORM}	repetitive peak output current		-	8	A
$P_{d(max)}$	maximum power dissipation		-	2.5	W
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

11. Thermal characteristics

Table 8: Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance junction to ambient	in free air	[1]	24	K/W
$R_{th(j-p)}$	thermal resistance junction to pin	in free air	[2]	16	K/W
$R_{th(j-c)}$	thermal resistance junction to case	in free air	[3]	3	K/W

[1] Measured in the application board.

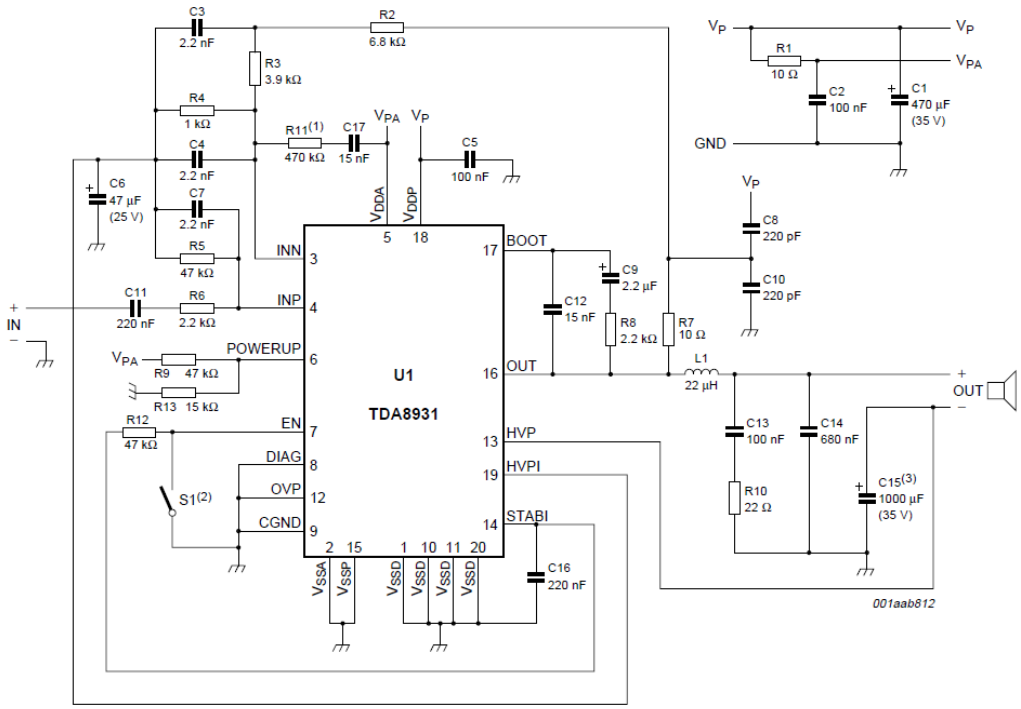
[2] V_p = 22 V; R_L = 4 Ω; V_{ripple} = 2 V (p-p); f_{ripple} = 100 Hz with feed-forward network (470 kΩ and 15 nF).

[3] Strongly depending on where you measure on the case.

13. Dynamic characteristics

Table 10: Characteristics
V_P = 22 V; T_{amb} = 25 °C; R_L = 4 Ω; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier; SE channel							
$P_{o(max)}$	maximum output power	R_L = 4 Ω; THD = 10 %	[1]				
		V_P = 26 V		21	22	-	W
		V_P = 22 V		15	16	-	W
		R_L = 8 Ω; THD = 10 %					
		V_P = 30 V		15	16	-	W
THD	total harmonic distortion	P_o = 1 W, f_i = 1 kHz	[1]	-	0.02	0.1	%
$V_{n(o)}$	noise output voltage	Operating mode; inputs shorted; gain = 20 dB, AES17 brick wall filter	[1]	-	128	150	µV
$G_{v(range)}$	gain adjust range		[1]	14	20	26	dB
η	efficiency	P_o = 15 W					
		V_p = 22 V; R_L = 4 Ω	[1]	87	89	-	%
		V_p = 30 V; R_L = 8 Ω	[1]	89	91	-	%
PWM output: pin OUT (see Figure 4)							
t_r	output voltage rise time			-	20	-	ns
t_f	output voltage fall time			-	20	-	ns
t_{dead}	dead time			-	0	-	ns
$t_{r(LH)}$	response time of transition from LOW-to-HIGH	$V_{i(dif)}$ = 70 mV		-	120	-	ns
		$V_{i(dif)}$ = 3.3 V		-	100	-	ns
$t_{r(HL)}$	response time of transition from HIGH-to-LOW	$V_{i(dif)}$ = 70 mV		-	120	-	ns
		$V_{i(dif)}$ = 3.3 V		-	100	-	ns
$t_{W(min)}$	minimum pulse width			-	150	-	ns
R_{DSon}	drain-source on-state resistance of output transistor			-	0.22	0.3	Ω



(1) Optional feed forward network to improve SVRR.

(2) Standby mode: S1 = closed; Operating mode: S1 = open.

(3) The low frequency gain is determined by the capacitor in series with the speaker. The cut-off frequency with a 4 Ω speaker and C15 = 1000 µF is 40 Hz.

Fig 5. Typical application diagram with TDA8931 supplied from an asymmetrical supply

14.1 Output power estimation

The output power, just before clipping, can be estimated using the following equation:

$$P_{o(1\%)} = \frac{\left(\frac{R_L}{R_L + R_{DSon} + R_{coil} + R_{ESR}} \times V_P\right)^2}{8 \times R_L} \quad (2)$$

Where:

$P_{o(1\%)}$ = output power just before clipping at THD = 1 %

R_L = load impedance

R_{DSon} = on-resistance power switch

R_{coil} = series resistance output coil

R_{ESR} = ESR of the single-ended capacitor

V_P = supply voltage ($V_{DDP} - V_{SSP}$)

Example: Substituting R_L = 4 Ω, R_{DSon} = 0.22 Ω (at T_j = 25 °C), R_{coil} = 0.045 Ω, R_{ESR} = 0.06 Ω and V_P = 22 V results in output power P_o = 12.9 W.

The output power at THD = 10 % can be estimated by:

$$P_{o(10\%)} = 1.25 \times P_{o(1\%)} \quad (3)$$

14.3 Low pass filter considerations

For a flat frequency response (second order Butterworth filter) it is necessary to change the LC-filter components (L1 and C14) according to the speaker impedance. Table 12 shows the required components values in case of a 4 W, 6 W or 8 W speaker impedance.

Table 12: Filter components values

Speaker impedance (Ω)	L1 value (µH)	C14 value (nF)
4	22	680
6	33	470
8	47	330