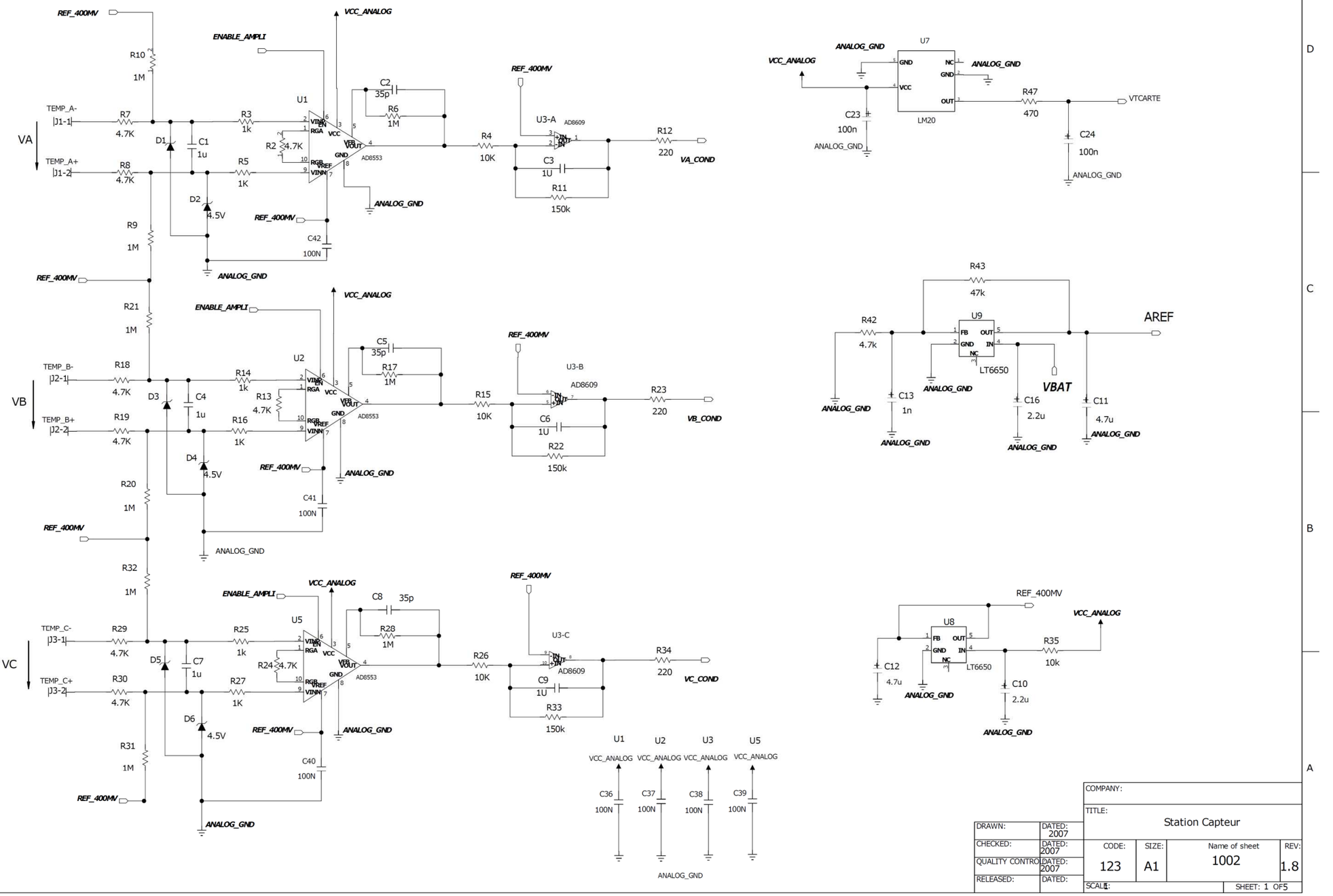
DOCUMENTATION

SOMMAIRE



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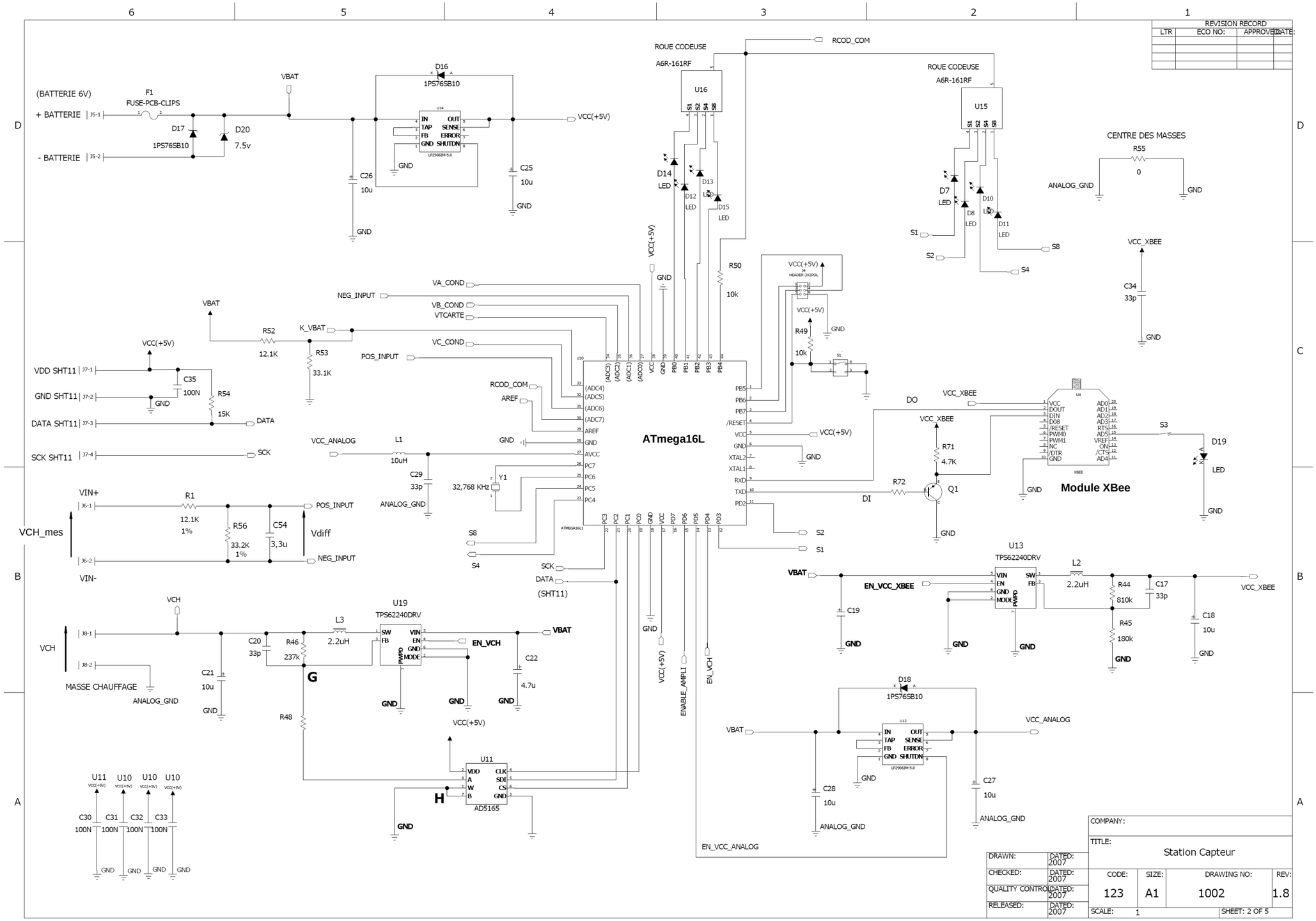
		SCALE:	SHEET: 1 OF5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LTR
ECO NO:
APPROVED
DATE:
(BATTERIE 6V)
F1
FUSE-PCB-CLIPS
+ BATTERIE
- BATTERIE
D17
1PS76SB10
D20
7.5v
VBAT
D16
1PS76SB10
U14
LP2996M-5.0
VCC(+5V)
C26
10u
C25
10u
GND
ROUE CODEUSE
A6R-161RF
U16
RCOD_COM
D14
LED
D12
LED
D13
LED
D15
LED
R50
10k
VCC(+5V)
ROUE CODEUSE
A6R-161RF
U15
D7
LED
D8
LED
D10
LED
D11
LED
S1
S2
S4
S8
CENTRE DES MASSES
R55
0
ANALOG_GND
VCC_XBEE
C34
33p
VA_COND
NEG_INPUT
VB_COND
VTCARTE
VC_COND
POS_INPUT
VBAT
R52
12.1K
K_VBAT
R53
33.1K
VCC(+5V)
VDD SHT11
GND SHT11
DATA SHT11
SCK SHT11
C35
100N
R54
15K
DATA
SCK
U10
ATmega16L
RCOD_COM
AREF
VCC_ANALOG
L1
10uH
C29
33p
ANALOG_GND
Y1
32,768 KHz
S8
S4
SCK
DATA
(SHT11)
S2
S1
VCC(+5V)
GND
EN_VCH
ENABLE_AMPLI
R49
10k
VCC_XBEE
DO
DI
R71
4.7K
R72
Q1
Module XBee
S3
D19
LED
VIN+
VIN-
VCH_mes
R1
12.1K
1%
R56
33.2K
1%
C54
3,3u
Vdiff
POS_INPUT
NEG_INPUT
U13
TPS62240DRV
L2
2.2uH
R44
810k
R45
180k
C17
33p
C18
10u
C19
VBAT
EN_VCC_XBEE
VCC_XBEE
VCH
MASSE CHAUFFAGE
ANALOG_GND
U19
TPS62240DRV
L3
2.2uH
C20
33p
R46
237k
C21
10u
C22
4.7u
R48
EN_VCH
VBAT
G
H
U11
AD5165
U11
U10
U10
U10
C30
C31
C32
C33
100N
D18
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Station Capteur
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DATED:
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CODE:
123
SIZE:
A1
DRAWING NO:
1002
REV:
1.8
SCALE:
1
SHEET: 2 OF 5

3.1 Mechanical Specifications

Model No.	Gage Height (mm)	Shield Height (mm)	Stem Diameter (mm)			TC Gap dX (mm)	NO. Pairs	Input Voltage (Volts)	Input Power (Watts)
			Min.	Typ.	Max.*				
Micro Flow Gages									
SGA2-ws	35	70	2.1	2.5	3.5	1.0	1	2.3	.05
SGA3-ws	35	70	2.75	3.0	4.0	1.0	1	2.3	.05
SGA5-ws	35	70	5	5.5	7	3.0	2	4.0	0.08
Stem Flow Gage									
SGA9-ws	70	180	8	9	10	4.0	2	4.0	0.10
SGA10-ws	70	180	9.5	10	13	4.0	2	4.0	0.10
SGA13-ws	70	180	12	13	16	4.0	2	4.0	0.15
SGB16-ws	70	200	15	16	19	5.0	2	4.5	0.20
SGB19-ws	130	250	18	19	23	5.0	2	4.5`	0.30
SGB25-ws	110	280	24	28	32	7.0	2	4.5	0.50
Trunk Gages									
SGB35-ws	255	460	32	41	45	10.0	4	6.0	0.90
SGB50-ws	305	505	45	50	65	10.0	8	6.0	1.4
SGA70-ws	410	610	65	70	90	13.0	8	6.0	1.6
SGA100-ws	460	660	100	110	125	15.0	8	8.5	4.0
SGA150-ws	900	1,129	150	110	165	20.0	8	9.0	4.0

Figure 3.1 Dynagage Mechanical Specifications

Heater input voltage D.C.
Measured at device terminals D (+), E (-)

Part Number	Min	Typ	Max	Unit
SGA3	2.2	2.5	2.7	V.
SGA5	3.5	4.0	4.5	V.
SGA9	3.5	4.0	5.0	V.
SGA10	3.5	4.0	5.0	V.
SGA13	3.5	4.0	5.0	V.
SGB16	3.5	4.5	5.0	V.
SGB19	3.5	4.5	5.0	V.
SGB25	3.5	4.0	5.0	V.
SGB35	4.5	5.5	7.0	V.
SGB50	4.5	5.5	7.0	V.
SGA70	5.0	6.0	7.0	V.
SGA100	6.0	8.5	10.0	V
SGA150	8.5	9.0	10.0	V.

Table 3.1 Recommended Heater Input Voltage

Heater Input power
Recommended for each; Pin = V*V/R

Part Number	Min	Typ	Max	Unit
SGA2	.04	.05	.06	W.
SGA3	.05	.06	.07	W.
SGA5	.05	.08	.10	W.
SGA9	.06	.12	.15	W.
SGA10	.06	.12	.15	W.
SGA13	.09	.17	.20	W.
SGB16	.10	.20	.25	W.
SGB19	.16	.30	.40	W.
SGB25	.26	.4	.5	W.
SGB35	.45	.75	1.2	W.
SGB50	.70	1.2	2.0	W.
SGA70	1.1	1.6	2.5	W
SGA100	2.0	4.0	5.5	W
SGA150	9.6	10.8	13.3	W

Table 3.2 Recommended Heater Input Power

Model	Min	Typ	Max	Units
SGA2	80	90	100	Ohm
SGA3	100	110	120	Ohm
SGA5	170	190	200	Ohm
SGA9	105	120	135	Ohm
SGA10	120	150	170	Ohm
SGA13	105	120	135	Ohm
SGB16	50	100	120	Ohm
SGB19	50	65	75	Ohm
SGB25	38	43	47	Ohm
SGB35	35	40	45	Ohm
SGB50	21	25	29	Ohm
SGA70	20	22	25	Ohm
SGA100	16	18	20	Ohm
SGA150				

Table 3.3 - Heater element impedances. A 10% variation from unit to unit is normal. An upgrade in design may change impedances without notice to improve compatibility.

Absolute maximum power & environmental limits	***MAX***	***MODEL***
Absolute maximum power applied to heater (D-E)	*0.2 Watt*	*SGA2, SGA3, SGA5*
If you exceed this specification it voids the Warranty.	*0.5 Watt*	*SGA 9, 10, 13, SGB16*
This specification is the maximum power which	*2.0 Watt*	*SGB19, SGB25*
can be applied without damage to the gage heater,	*5.0 Watt*	*SGB35, SGB50*
NOT the maximum you should apply to the plant.	*10. Watt*	*SGA70, SGA100*
Maximum operating temperature	*45 C.*	*All*
Maximum storage temperature	60 C.	Models

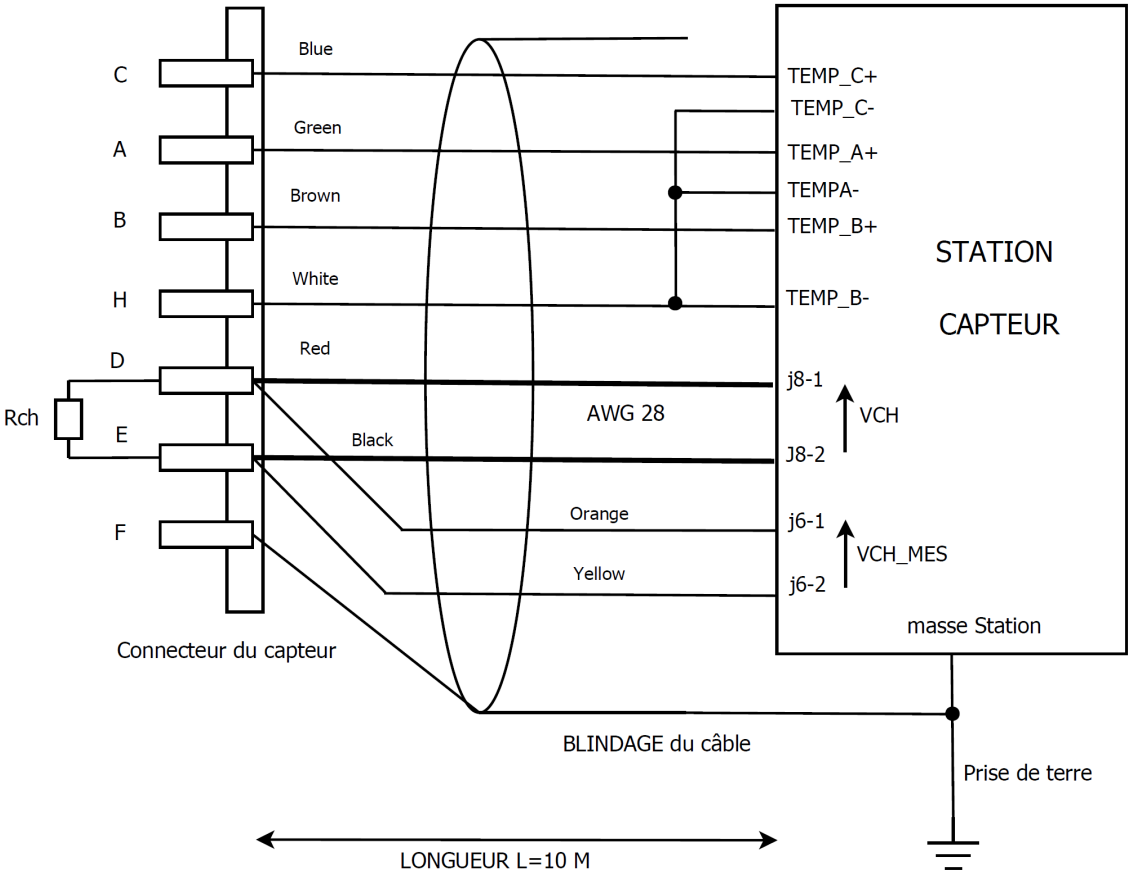


Fig. 3.2 Interconnexion du capteur à la Station Capteur

256-Position, Ultralow Power 1.8 V Logic-Level Digital Potentiometer

AD5165

FEATURES

- Ultralow standby power I_{DD} = 50 nA typical
- 256-position
- End-to-end resistance 100 kΩ
- Logic high voltage 1.8 V
- Power supply 2.7 V to 5.5 V
- Low temperature coefficient 35 ppm/°C
- Compact thin 8-lead TSOT-8 (2.9 mm × 2.8 mm) package
- Simple 3-wire digital interface
- Wide operating temperature −40°C to +125°C
- Pin-to-pin compatible to AD5160 with CS inverted

APPLICATIONS

- Battery-operated electronics adjustment
- Remote utilities meter adjustment
- Mechanical potentiometer replacement
- Transducer circuit adjustment
- Automotive electronics adjustment
- Gain control and offset adjustment
- System calibration
- VCXO adjustment

GENERAL OVERVIEW

The AD5165 provides a compact 2.9 mm × 2.8 mm packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance. The AD5165's supply voltage requirement is 2.7 V to 5.5 V, but its logic voltage requirement is 1.8 V to V_{DD}. The AD5165 consumes very low quiescent power during standby mode and is ideal for battery-operated applications.

Wiper settings are controlled through a simple 3-wire interface. The interface is similar to the SPI® digital interface except for the inverted chip-select function that minimizes logic power consumption in the idling state. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the wiper register.

FUNCTIONAL BLOCK DIAGRAM

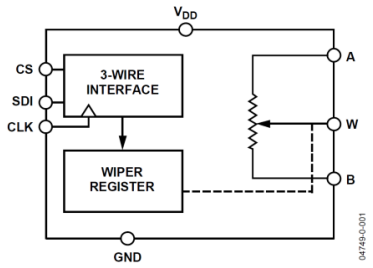


Figure 1.

PIN CONFIGURATION

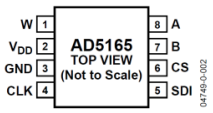


Figure 2.

TYPICAL APPLICATION

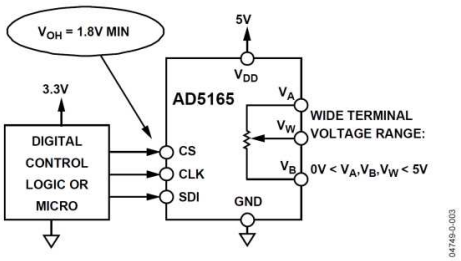


Figure 3.

3-WIRE DIGITAL INTERFACE

Note that in the AD5165 data is loaded MSB first.

Table 5. AD5165 Serial Data-Word Format

B7	B6	B5	B4	B3	B2	B1	B0
D7 MSB 2^7	D6	D5	D4	D3	D2	D1	D0 LSB 2^0

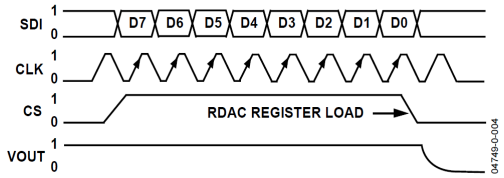


Figure 34. 3-Wire Digital Interface Timing Diagram
(V_A = 5 V, V_B = 0 V, $V_W = V_{OUT}$)

THEORY OF OPERATION

The AD5165 is a 256-position digitally controlled variable resistor (VR) device.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 100 kΩ. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

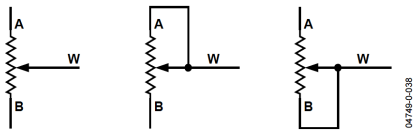


Figure 36. Rheostat Mode Configuration

Assuming that a 100 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between terminals W and B. The second connection is the first tap point, which corresponds to 490 Ω ($R_{WB} = R_{AB}/256 + 2 \times R_W = 390\ \Omega + 2 \times 50\ \Omega$) for data 0x01. The third connection is the next tap point, representing 880 Ω (2 × 390 Ω + 2 × 50 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 100,100 Ω ($R_{AB} + 2 \times R_W$).

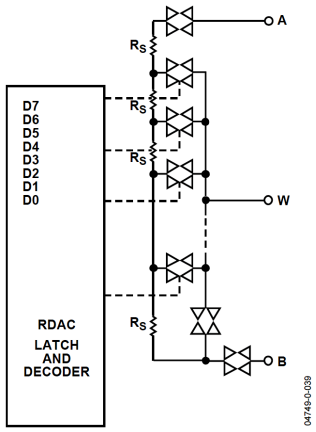


Figure 37. AD5165 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \qquad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 100 kΩ and the A terminal is open circuited, the following output resistance R_{WB} is set for the indicated RDAC latch codes.

Table 6. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
255	99 710	Full scale (R_{AB} – 1 LSB + R_W)
128	50 100	Midscale
1	490	1 LSB
0	100	Zero scale (wiper contact resistance)

Note that, in the zero-scale condition, a finite wiper resistance of 100 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \qquad (2)$$

For R_{AB} = 100 kΩ with the B terminal open circuited, the following output resistance R_{WA} is set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WA} Resistance

D (Dec.)	R_{WA} (Ω)	Output State
255	490	Full scale
128	50 100	Midscale
1	99 710	1 LSB
0	100 100	Zero scale

Typical device-to-device matching is process-lot dependent and may vary by up to ±20%. Because the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 35 ppm/°C temperature coefficient.

2.25 MHz 300 mA Step Down Converter in 2x2SON/TSOT23 Package

FEATURES

- High Efficiency Step Down Converter
- Output Current up to 300 mA
- V_{IN} Range From 2 V to 6 V for Li-Ion Batteries With Extended Voltage Range
- 2.25 MHz Fixed Frequency Operation
- Power Save Mode at Light Load Currents
- Output Voltage Accuracy in PWM Mode ±1.5%
- Adjustable Output Voltage from 0.6 V to V_{IN}
- Typical 15 µA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Available in a TSOT23 and 2×2×0,8 mm SON
- Allows < 1 mm Solution Height

APPLICATIONS

- Bluetooth™ Headset
- Cell Phones, Smart-phones
- WLAN
- PDAs, Pocket PCs
- Low Power DSP Supply
- Portable Media Players
- Digital Cameras

DESCRIPTION

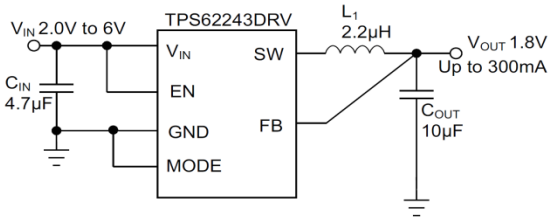
The TPS62240 device is a high efficiency synchronous step down dc-dc converter optimized for battery powered portable applications. It provides up to 300 mA output current from a single Li-Ion cell and is ideal to power portable applications like mobile phones and other portable equipment..

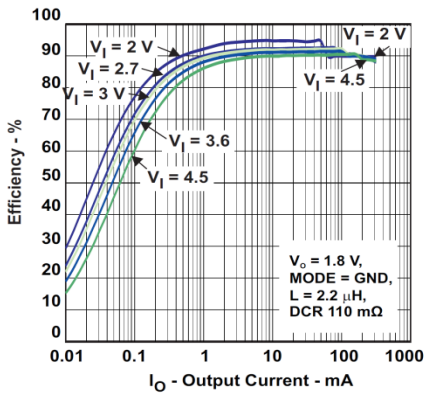
With an input voltage range of 2 V to 6 V, the device supports applications powered by Li-Ion batteries with extended voltage range, two- and three-cell alkaline, 3.3-V and 5-V input voltage rails.

The TPS62240 operates at 2.25 MHz fixed switching frequency and enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range.

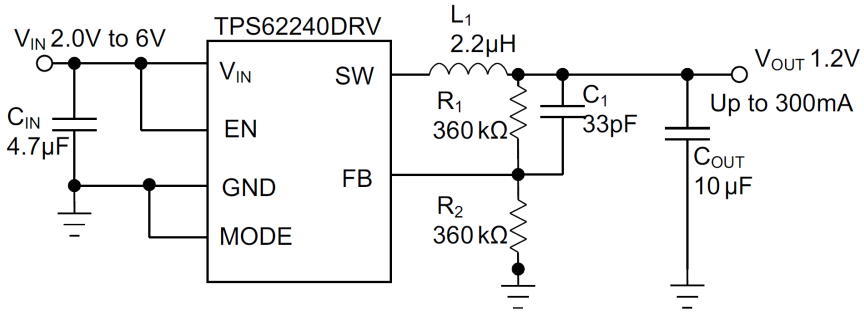
The Power Save Mode is optimized for low output voltage ripple. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA. TPS62240 allows the use of small inductors and capacitors to achieve a small solution size.

The TPS62240 is available in a 5-pin TSOT23 and 6-pin 2mm×2mm SON package.





APPLICATION INFORMATION



OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

with an internal reference voltage V_{REF} typical 0.6 V.

Tableau des valeurs de résistances normalisées E96

E96 (±1%) : 100 - 102 - 105 - 107 - 110 - 113 - 115
118 - 121 - 124 - 127 - 130 - 133 - 137 - 140
143 - 147 - 150 - 154 - 158 - 162 - 165 - 169
174 - 178 - 182 - 187 - 191 - 196 - 200 - 205
210 - 215 - 221 - 226 - 232 - 237 - 243 - 249
255 - 261 - 267 - 274 - 280 - 287 - 294 - 301
309 - 316 - 324 - 332 - 340 - 348 - 357 - 365
374 - 383 - 392 - 402 - 412 - 422 - 432 - 442
453 - 464 - 475 - 487 - 499 - 511 - 523 - 536
549 - 562 - 576 - 590 - 604 - 619 - 634 - 649
665 - 681 - 698 - 715 - 732 - 750 - 768 - 787
806 - 825 - 845 - 866 - 887 - 909 - 931 - 953 - 976

Table de correspondance AWG

Electronics Technical Information

AWG Conductor Chart

COPPER CONDUCTOR DATA

The conductors used by General Cable meet the applicable requirements of ASTM specifications B-3, B-33, B-172, B-173, B-174 and B-286 and Federal Specification QQ-W-343.

The following data covers the more commonly used conductor constructions in the electrical and electronics industry. Special constructions, not shown, are available or can be designed to meet specific requirements. It is suggested that the General Cable Product Engineering Department be contacted before a specification is finalized.

AWG	STRANDING	TYPE STRANDING	DIAMETER(4)		AREA		WEIGHT		D.C. RESISTANCE 20°C(2)				BREAK STR. LBS
									TIN COATING(3)		BARE OF SILVER COATING		
			in	mm	circ. mils	sq. mm	lbs/Mft	kg/km	Ω/Mft	Ω/km	Ω/Mft	Ω/km	
32	7/40	Co or Bu	.0096	.254	100	.051	.21	.31	176.00	577.00	164.00	538.00	1.986
30	Solid	–	.010	.254	100	.051	.30	.45	113.00	371.00	104.00	340.00	3.157
	7/38	Bu	.012	.305	112	.057	.35	.52	106.00	348.00	92.60	303.00	
28	Solid	–	.01264	.321	159	.081	.48	.72	70.80	232.00	65.30	214.00	5.020
	7/36	Co	.015	.381	175	.089	.55	.82	67.50	221.00	59.30	194.00	
27	Solid	–	.0142	.361	202	.102	.61	.91	55.60	182.00	51.40	169.00	6.331
	7/35	Co or Bu	.017	.432	220	.111	.69	1.04	53.80	176.00	–	–	
26	Solid	–	.016	.404	253	.128	.77	1.14	44.50	146.00	41.00	135.00	7.983
	7/34	Co or Bu	.019	.483	278	.141	.87	1.29	42.50	139.00	37.30	122.00	
	10/36	Bu	.0193	.490	250	.127	.78	1.15	47.30	155.00	40.40	133.00	
	19/38	Bu or Co	.021	.533	304	.154	.97	1.44	38.90	128.00	34.10	112.00	

(1) Bu - Bunched; Co - Concentric; Eq - Equilay; Ro - Rope; Un - Unilay
(2) Typical D.C. Resistance values for uninsulated wires. Multiply by 1.04 for typical values after insulation
(3) Values are for tinned, heavy tinned, prefused, overcoated or topcoated conductors
(4) Does not meet UL conductor stranding requirements

Analog to Digital Converter

Features

- **10-bit Resolution**
- **0.5 LSB Integral Non-linearity**
- **±2 LSB Absolute Accuracy**
- **13 µs- 260 µs Conversion Time**
- **Up to 15 kSPS at Maximum Resolution**
- **8 Multiplexed Single Ended Input Channels**
- **7 Differential Input Channels**
- **2 Differential Input Channels with Optional Gain of 10x and 200x**
- **Optional Left adjustment for ADC Result Readout**
- **0 - V_{CC} ADC Input Voltage Range**
- **Selectable 2.56V ADC Reference Voltage**
- **Free Running or Single Conversion Mode**
- **ADC Start Conversion by Auto Triggering on Interrupt Sources**
- **Interrupt on ADC Conversion Complete**
- **Sleep Mode Noise Canceler**

The ATmega16 features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel Analog Multiplexer which allows 8 single-ended voltage inputs constructed from the pins of Port A. The single-ended voltage inputs refer to 0V (GND).

The device also supports 16 differential voltage input combinations. Two of the differential inputs (ADC1, ADC0 and ADC3, ADC2) are equipped with a programmable gain stage, providing amplification steps of 0 dB (1x), 20 dB (10x), or 46 dB (200x) on the differential input voltage before the A/D conversion. Seven differential analog input channels share a common negative terminal (ADC1), while any other ADC input can be selected as the positive input terminal. If 1x or 10x gain is used, 8-bit resolution can be expected. If 200x gain is used, 7-bit resolution can be expected.

The ADC contains a Sample and Hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 98.

The ADC has a separate analog supply voltage pin, AVCC. AVCC must not differ more than ±0.3V from V_{CC}. See the paragraph “ADC Noise Canceler” on page 211 on how to connect this pin.

Internal reference voltages of nominally 2.56V or AVCC are provided On-chip. The voltage reference may be externally decoupled at the AREF pin by a capacitor for better noise performance.

ADC Conversion Result

After the conversion is complete (ADIF is high), the conversion result can be found in the ADC Result Registers (ADCL, ADCH).

For single ended conversion, the result is

$$ADC = \frac{V_{IN} \cdot 1024}{V_{REF}}$$

where V_{IN} is the voltage on the selected input pin and V_{REF} the selected voltage reference (see Table 83 on page 217 and Table 84 on page 218). 0x000 represents ground, and 0x3FF represents the selected reference voltage minus one LSB.

If differential channels are used, the result is

$$ADC = \frac{(V_{POS} - V_{NEG}) \cdot GAIN \cdot 512}{V_{REF}}$$

where V_{POS} is the voltage on the positive input pin, V_{NEG} the voltage on the negative input pin, GAIN the selected gain factor, and V_{REF} the selected voltage reference. The result is presented in two’s complement form, from 0x200 (-512d) through 0x1FF (+511d). Note that if the user wants to perform a quick polarity check of the results, it is sufficient to read the MSB of the result (ADC9 in ADCH). If this bit is one, the result is negative, and if this bit is zero, the result is positive. Figure 111 shows the decoding of the differential input range.

Table 82 shows the resulting output codes if the differential input channel pair (ADCn - ADCm) is selected with a gain of GAIN and a reference voltage of V_{REF}.

ADC Multiplexer Selection Register – ADMUX

Bit	7	6	5	4	3	2	1	0	
	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	ADMUX
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7:6 – REFS1:0: Reference Selection Bits**

These bits select the voltage reference for the ADC, as shown in Table 83. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set). The internal voltage reference options may not be used if an external reference voltage is being applied to the AREF pin.

Table 83. Voltage Reference Selections for ADC

REFS1	REFS0	Voltage Reference Selection
0	0	AREF, Internal Vref turned off
0	1	AVCC with external capacitor at AREF pin
1	0	Reserved
1	1	Internal 2.56V Voltage Reference with external capacitor at AREF pin

- **Bit 5 – ADLAR: ADC Left Adjust Result**

The ADLAR bit affects the presentation of the ADC conversion result in the ADC Data Register. Write one to ADLAR to left adjust the result. Otherwise, the result is right adjusted. Changing the ADLAR bit will affect the ADC Data Register immediately, regardless of any ongoing conversions. For a complete description of this bit, see "The ADC Data Register – ADCL and ADCH" on page 220.

- **Bits 4:0 – MUX4:0: Analog Channel and Gain Selection Bits**

The value of these bits selects which combination of analog inputs are connected to the ADC. These bits also select the gain for the differential channels. See Table 84 for details. If these bits are changed during a conversion, the change will not go in effect until this conversion is complete (ADIF in ADCSRA is set).

Table 84. Input Channel and Gain Selections

MUX4..0	Single Ended Input	Positive Differential Input	Negative Differential Input	Gain
00000	ADC0	N/A		
00001	ADC1			
00010	ADC2			
00011	ADC3			
00100	ADC4			
00101	ADC5			
00110	ADC6			
00111	ADC7			
01000	N/A	ADC0	ADC0	10x
01001		ADC1	ADC0	10x
01010		ADC0	ADC0	200x
01011		ADC1	ADC0	200x
01100		ADC2	ADC2	10x
01101		ADC3	ADC2	10x
01110		ADC2	ADC2	200x
01111		ADC3	ADC2	200x
10000		ADC0	ADC1	1x
10001		ADC1	ADC1	1x
10010		ADC2	ADC1	1x
10011		ADC3	ADC1	1x
10100		ADC4	ADC1	1x
10101		ADC5	ADC1	1x
10110		ADC6	ADC1	1x
10111		ADC7	ADC1	1x
11000		ADC0	ADC2	1x
11001		ADC1	ADC2	1x
11010		ADC2	ADC2	1x
11011		ADC3	ADC2	1x
11100		ADC4	ADC2	1x

USART Baud Rate Registers – UBRRL and UBRRH

Bit	15	14	13	12	11	10	9	8	
	URSEL	–	–	–	UBRR[11:8]				UBRRH
	UBRR[7:0]								UBRRL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

The UBRRH Register shares the same I/O location as the UCSRC Register. See the “Accessing UBRRH/ UCSRC Registers” on page 162 section which describes how to access this register.

- **Bit 15 – URSEL: Register Select**

This bit selects between accessing the UBRRH or the UCSRC Register. It is read as zero when reading UBRRH. The URSEL must be zero when writing the UBRRH.

- **Bit 14:12 – Reserved Bits**

These bits are reserved for future use. For compatibility with future devices, these bit must be written to zero when UBRRH is written.

- **Bit 11:0 – UBRR11:0: USART Baud Rate Register**

This is a 12-bit register which contains the USART baud rate. The UBRRH contains the four most significant bits, and the UBRRL contains the 8 least significant bits of the USART baud rate. Ongoing transmissions by the transmitter and receiver will be corrupted if the baud rate is changed. Writing UBRRL will trigger an immediate update of the baud rate prescaler.

Examples of Baud Rate Setting

For standard crystal and resonator frequencies, the most commonly used baud rates for asynchronous operation can be generated by using the UBRR settings in Table 68. UBRR values which yield an actual baud rate differing less than 0.5% from the target baud rate, are bold in the table. Higher error ratings are acceptable, but the receiver will have less noise resistance when the error ratings are high, especially for large serial frames (see “Asynchronous Operational Range” on page 159). The error values are calculated using the following equation:

$$\text{Error}[\%] = \left(\frac{\text{BaudRate}_{\text{Closest Match}}}{\text{BaudRate}} - 1\right) \bullet 100\%$$

Table 69. Examples of UBRR Settings for Commonly Used Oscillator Frequencies (Continued)

Baud Rate (bps)	f_{osc} = 3.6864 MHz				f_{osc} = 4.0000 MHz				f_{osc} = 7.3728 MHz			
	U2X = 0		U2X = 1		U2X = 0		U2X = 1		U2X = 0		U2X = 1	
	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error	UBRR	Error
2400	95	0.0%	191	0.0%	103	0.2%	207	0.2%	191	0.0%	383	0.0%
4800	47	0.0%	95	0.0%	51	0.2%	103	0.2%	95	0.0%	191	0.0%
9600	23	0.0%	47	0.0%	25	0.2%	51	0.2%	47	0.0%	95	0.0%
14.4k	15	0.0%	31	0.0%	16	2.1%	34	-0.8%	31	0.0%	63	0.0%
19.2k	11	0.0%	23	0.0%	12	0.2%	25	0.2%	23	0.0%	47	0.0%
28.8k	7	0.0%	15	0.0%	8	-3.5%	16	2.1%	15	0.0%	31	0.0%
38.4k	5	0.0%	11	0.0%	6	-7.0%	12	0.2%	11	0.0%	23	0.0%
57.6k	3	0.0%	7	0.0%	3	8.5%	8	-3.5%	7	0.0%	15	0.0%
76.8k	2	0.0%	5	0.0%	2	8.5%	6	-7.0%	5	0.0%	11	0.0%
115.2k	1	0.0%	3	0.0%	1	8.5%	3	8.5%	3	0.0%	7	0.0%
230.4k	0	0.0%	1	0.0%	0	8.5%	1	8.5%	1	0.0%	3	0.0%
250k	0	-7.8%	1	-7.8%	0	0.0%	1	0.0%	1	-7.8%	3	-7.8%
0.5M	–	–	0	-7.8%	–	–	0	0.0%	0	-7.8%	1	-7.8%
1M	–	–	–	–	–	–	–	–	–	–	0	-7.8%
Max (1)	230.4 Kbps		460.8 Kbps		250 Kbps		0.5 Mbps		460.8 Kbps		921.6 Kbps	

1. UBRR = 0, Error = 0.0%

Specifications

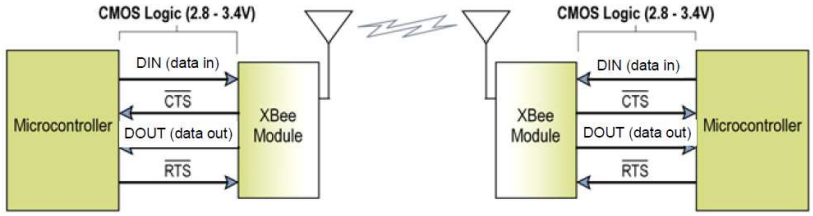
Specifications of the XBee®/XBee-PRO® ZB RF Module

Specification	XBee	XBee-PRO (S2)	XBee-PRO (S2B)
Performance			
Indoor/Urban Range	up to 133 ft. (40 m)	Up to 300 ft. (90 m), up to 200 ft (60 m) international variant	Up to 300 ft. (90 m), up to 200 ft (60 m) international variant
Outdoor RF line-of-sight Range	up to 400 ft. (120 m)	Up to 2 miles (3200 m), up to 5000 ft (1500 m) international variant	Up to 2 miles (3200 m), up to 5000 ft (1500 m) international variant
Transmit Power Output	2mW (+3dBm), boost mode enabled 1.25mW (+1dBm), boost mode disabled	50mW (+17 dBm) 10mW (+10 dBm) for International variant	63mW (+18 dBm) 10mW (+10 dBm) for International variant
RF Data Rate	250,000 bps	250,000 bps	250,000 bps
Data Throughput	up to 35000 bps (see chapter 4)	up to 35000 bps (see chapter 4)	up to 35000 bps (see chapter 4)
Serial Interface Data Rate (software selectable)	1200 bps - 1 Mbps (non-standard baud rates also supported)	1200 bps - 1 Mbps (non-standard baud rates also supported)	1200 bps - 1 Mbps (non-standard baud rates also supported)
Receiver Sensitivity	-96 dBm, boost mode enabled -95 dBm, boost mode disabled	-102 dBm	-102 dBm
Power Requirements			
Supply Voltage	2.1 - 3.6 V	3.0 - 3.4 V	2.7 - 3.6 V
Operating Current (Transmit, max output power)	40mA (@ 3.3 V, boost mode enabled) 35mA (@ 3.3 V, boost mode disabled)	295mA (@3.3 V) 170mA (@3.3 V) international variant	205mA, up to 220 mA with programmable variant (@3.3 V) 117mA, up to 132 mA with programmable variant (@3.3 V), International variant
Operating Current (Receive))	40mA (@ 3.3 V, boost mode enabled) 38mA (@ 3.3 V, boost mode disabled)	45 mA (@3.3 V)	47 mA, up to 62 mA with programmable variant (@3.3 V)
Idle Current (Receiver off)	15mA	15mA	15mA
Power-down Current	< 1 uA @ 25°C	3.5 µA typical @ 25°C	3.5 µA typical @ 25°C
General			
Operating Frequency Band	ISM 2.4 GHz	ISM 2.4 GHz	ISM 2.4 GHz
Dimensions	0.960" x 1.087" (2.438cm x 2.761cm)	0.960 x 1.297 (2.438cm x 3.294cm)	0.960 x 1.297 (2.438cm x 3.294cm)
Operating Temperature	-40 to 85° C (industrial)	-40 to 85° C (industrial)	-40 to 85° C (industrial)
Antenna Options	Integrated Whip, Chip, RPSMA, or U.FL Connector	Integrated Whip, Chip, RPSMA, or U.FL Connector	Integrated Whip,PCB Embedded Trace, RPSMA, or U.FL Connector
Networking & Security			
Supported Network Topologies	Point-to-point, Point-to-multipoint, Peer-to-peer, and Mesh	Point-to-point, Point-to-multipoint, Peer-to-peer, and Mesh	Point-to-point, Point-to-multipoint, Peer-to-peer, and Mesh
Number of Channels	16 Direct Sequence Channels	14 Direct Sequence Channels	15 Direct Sequence Channels
Channels	11 to 26	11 to 24	11 to 25
Addressing Options	PAN ID and Addresses, Cluster IDs and Endpoints (optional)	PAN ID and Addresses, Cluster IDs and Endpoints (optional)	PAN ID and Addresses, Cluster IDs and Endpoints (optional)
Agency Approvals			
United States (FCC Part 15.247)	FCC ID: OUR-XBEE2	FCC ID: MCQ-XBEEPRO2	FCC ID: MCQ-PROS2B
Industry Canada (IC)	IC: 4214A-XBEE2	IC: 1846A-XBEEPRO2	IC: 1846A-PROS2B
Europe (CE)	ETSI	ETSI (International variant)	ETSI (10 mW max)

UART Data Flow

Devices that have a UART interface can connect directly to the pins of the RF module as shown in the figure below.

System Data Flow Diagram in a UART-interfaced environment
(Low-asserted signals distinguished with horizontal line over signal name.)

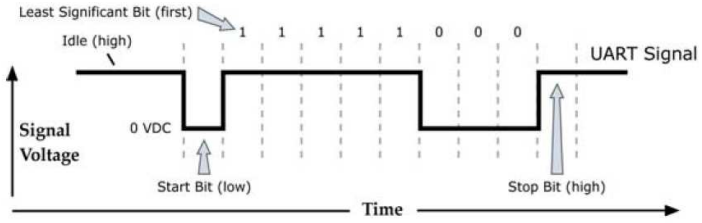


Serial Data

Data enters the module UART through the DIN (pin 3) as an asynchronous serial signal. The signal should idle high when no data is being transmitted.

Each data byte consists of a start bit (low), 8 data bits (least significant bit first) and a stop bit (high). The following figure illustrates the serial bit pattern of data passing through the module.

UART data packet 0x1F (decimal number "31") as transmitted through the RF module
Example Data Format is 8-N-1 (bits - parity - # of stop bits)



Serial communications depend on the two UARTs (the microcontroller's and the RF module's) to be configured with compatible settings (baud rate, parity, start bits, stop bits, data bits).

RF Interfacing

RF Interfacing Commands

AT Command	Name and Description	Node Type[1]	Parameter Range	Default
PL	**Power Level**. Select/Read the power level at which the RF module transmits conducted power. For XBee-PRO (S2B) Power Level 4 is calibrated and the other power levels are approximate.	CRE	**XBee** (boost mode disabled) 0 = -8 dBm 1 = -4 dBm 2 = -2 dBm 3 = 0 dBm 4 = +2 dBm **XBee-PRO (S2)** 4 = 17 dBm **XBee-PRO (S2) (International Variant)** 4 = 10dBm **XBee-PRO (S2B)** (Boost mode enabled) 4 = 18dBM 3 = 16dBm 2 = 14dBm 1 = 12dBm 0 = 10dBm **XBee-PRO (S2B) (International Variant)** (Boost mode enabled) 4 = 10dBm 3 = 8dBm 2 = 6dBm 1 = 4dBm 0 = 2dBm	4

Codes ASCII

Table des caractères ASCII de base

- Les codes 0 à 31 ne sont pas des caractères. On les appelle *caractères de contrôle* car ils permettent de faire des actions telles que:
  - retour à la ligne (CR)
  - Bip sonore (BEL)
- Les codes 65 à 90 représentent les majuscules
- Les codes 97 à 122 représentent les minuscules

Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char
0	00	Null	32	20	Space	64	40	@	96	60	`
1	01	Start of heading	33	21	!	65	41	A	97	61	a
2	02	Start of text	34	22	"	66	42	B	98	62	b
3	03	End of text	35	23	#	67	43	C	99	63	c
4	04	End of transmit	36	24	$	68	44	D	100	64	d
5	05	Enquiry	37	25	%	69	45	E	101	65	e
6	06	Acknowledge	38	26	&	70	46	F	102	66	f
7	07	Audible bell	39	27	'	71	47	G	103	67	g
8	08	Backspace	40	28	(	72	48	H	104	68	h
9	09	Horizontal tab	41	29	)	73	49	I	105	69	i
10	0A	Line feed	42	2A	*	74	4A	J	106	6A	j
11	0B	Vertical tab	43	2B	+	75	4B	K	107	6B	k
12	0C	Form feed	44	2C	,	76	4C	L	108	6C	l
13	0D	Carriage return	45	2D	-	77	4D	M	109	6D	m
14	0E	Shift out	46	2E	.	78	4E	N	110	6E	n
15	0F	Shift in	47	2F	/	79	4F	O	111	6F	o
16	10	Data link escape	48	30	0	80	50	P	112	70	p
17	11	Device control 1	49	31	1	81	51	Q	113	71	q
18	12	Device control 2	50	32	2	82	52	R	114	72	r
19	13	Device control 3	51	33	3	83	53	S	115	73	s
20	14	Device control 4	52	34	4	84	54	T	116	74	t
21	15	Neg. acknowledge	53	35	5	85	55	U	117	75	u
22	16	Synchronous idle	54	36	6	86	56	V	118	76	v
23	17	End trans. block	55	37	7	87	57	W	119	77	w
24	18	Cancel	56	38	8	88	58	X	120	78	x
25	19	End of medium	57	39	9	89	59	Y	121	79	y
26	1A	Substitution	58	3A	:	90	5A	Z	122	7A	z
27	1B	Escape	59	3B	;	91	5B	[	123	7B	{
28	1C	File separator	60	3C	<	92	5C	\	124	7C	|
29	1D	Group separator	61	3D	=	93	5D	]	125	7D	}
30	1E	Record separator	62	3E	>	94	5E	^	126	7E	~
31	1F	Unit separator	63	3F	?	95	5F	_	127	7F	□

Extraits du programme de gestion d'une Station Capteur

```
/*****************************************************
Project : Flux de sève
Version : StationCapteur 1.00
Date    : 18/04/2007
Chip type           : ATmega16L
Program type        : Application
Clock frequency     : 4,000000 MHz
Memory model        : Small
External SRAM size  : 0
Data Stack size     : 256
*****************************************************/
#include <mega16.h>
#include <stdio.h> // Standard Input/Output functions
.....
void configXBee(void) ;
……..
// USART Receiver buffer
……
#define RX_BUFFER_SIZE 104
char rx_buffer[RX_BUFFER_SIZE];
unsigned char rx_wr_index;

// This flag is set on USART Receiver buffer overflow
bit rx_buffer_overflow;

// USART Receiver interrupt service routine
interrupt [USART_RXC] void usart_rx_isr(void)
{
char status,data;
status=UCSRA;
data=UDR;
if ((status & (FRAMING_ERROR | PARITY_ERROR | DATA_OVERRUN))==0) // si pas d'erreurs sur le mot reçu
  {
  rx_buffer[rx_wr_index]=data;
  rx_wr_index++;
  if (rx_wr_index == RX_BUFFER_SIZE)
    {
    rx_wr_index=0;
    rx_buffer_overflow=1;
    }
  };
}
……
void main(void)
{
……
}
void configXBee(void)
  {
        command();      //Entrée en mode cmd.
        delay_ms(100);
        printf("ATDH0\r"); //Config adresse destination
        delay_ms(100);
        printf("ATDL0\r"); //Config adresse destination
        delay_ms(100);
        printf("ATMY2\r"); //config adresse source
        delay_ms(100);
        printf("ATPL4\r"); //config puissance d'émission
        delay_ms(100);
        ……
        printf("ATWR\r"); //Sauvegarde modifications
        delay_ms(100);
        printf("ATCN \r"); //Sortie du mode cmd
        delay_ms(3000);
        …….
        return; }……
```