Calculateur HDI

Dossier de documentation technique : DT

SAB C167 CS
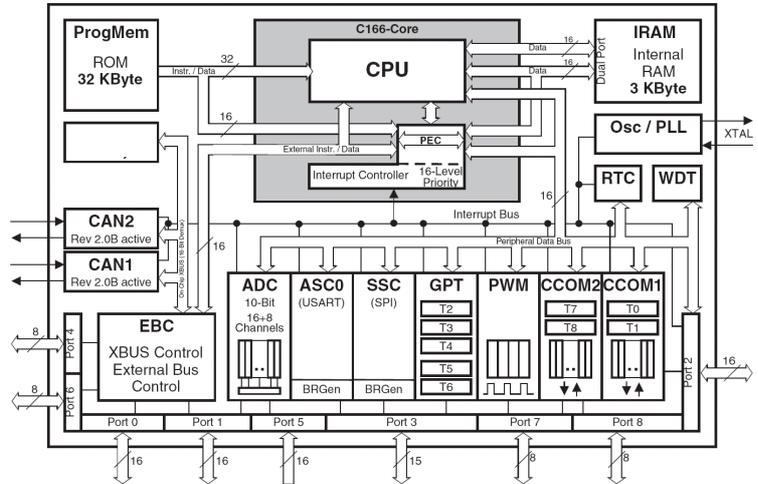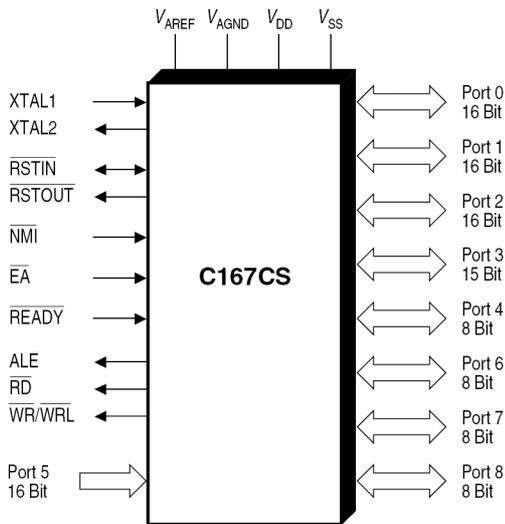
External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

		BTYP
16-/18-/20-/24-bit Addresses	8-bit Data, Demultiplexed	0 0
16-/18-/20-/24-bit Addresses	8-bit Data, Multiplexed	0 1
16-/18-/20-/24-bit Addresses	16-bit Data, Multiplexed	1 0
16-/18-/20-/24-bit Addresses	16-bit Data, Demultiplexed	1 1

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively.

In the multiplexed bus modes both addresses and data use PORT0 for input/output.

10-BIT ADC CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{ADC}	ADC clock frequency		0.4		2	MHz
V_{AREF}	Analog reference voltage [2]		$0.7 * V_{DD}$		5.5	V
V_{AIN}	Conversion voltage range [3]		V_{SSA}		V_{AREF}	
I_L	Input leakage current for analog input	$-40°C \leq T_A \leq 85°C$ range			±250	nA
		Other T_A ranges			±1	μA
C_{ADC}	Internal sample and hold capacitor			12		pF
t_{STAB}	Stabilization time after ADC enable			0 [5]		μs
t_{ADC}	Conversion time (Sample+Hold)	f_{CPU}=8MHz, SPEED=0 f_{ADC}=2MHz		7.5		
	- No of sample capacitor loading cycles - No. of Hold conversion cycles			4 11		$1/f_{ADC}$

ADDRSEL4
Address Select Register 4   **Reset value: 0000$_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					RGSAD								RGSZ		
					rw								rw		
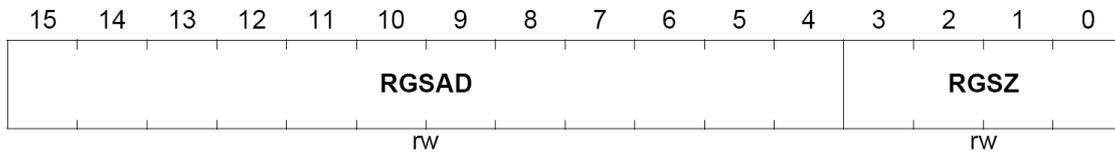
Bit	Function
RGSZ	**Range Size Selection** Defines the size of the address area controlled by the respective BUSCONx/ADDRSELx register pair. See **Table 9-6**.
RGSAD	**Range Start Address** Defines the upper bits of the start address of the respective address area. See **Table 9-6**.

Definition of Address Areas

The four register pairs BUSCON4/ADDRSEL4 … BUSCON1/ADDRSEL1 allow to define 4 separate address areas within the address space of the C167CR. Within each of these address areas external accesses can be controlled by one of the four different bus modes, independent of each other and of the bus mode specified in register BUSCON0.

Each ADDRSELx register in a way cuts out an address window, within which the parameters in register BUSCONx are used to control external accesses. The range start address of such a window defines the upper address bits, which are not used within the address window of the specified size (see **Table 9-6**). For a given window size only those upper address bits of the start address are used (marked "R"), which are not implicitly used for addresses inside the window. The lower bits of the start address (marked "x") are disregarded.

Table 9-6   Address Window Definition

Bit field RGSZ	Resulting Window Size	Relevant Bits (R) of Start Addr. (A12 …)
0 0 0 0	4 KByte	R R R R R R R R R R R R
0 0 0 1	8 KByte	R R R R R R R R R R R x
0 0 1 0	16 KByte	R R R R R R R R R R x x
0 0 1 1	32 KByte	R R R R R R R R R x x x
0 1 0 0	64 KByte	R R R R R R R R x x x x
0 1 0 1	128 KByte	R R R R R R R x x x x x
0 1 1 0	256 KByte	R R R R R R x x x x x x
0 1 1 1	512 KByte	R R R R R x x x x x x x
1 0 0 0	1 MByte	R R R R x x x x x x x x
1 0 0 1	2 MByte	R R R x x x x x x x x x
1 0 1 0	4 MByte	R R x x x x x x x x x x
1 0 1 1	8 MByte	R x x x x x x x x x x x
1 1 x x	Reserved.	

AMD ◢

Am29F400B

4 Megabit (512 K x 8-Bit/256 K x 16-Bit)
CMOS 5.0 Volt-only Boot Sector Flash Memory

PIN CONFIGURATION

A0–A17	=	18 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin, active low
RY/BY#	=	Ready/Busy# output
V_{CC}	=	+5.0 V single power supply (see Product Selector Guide for device speed ratings and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL
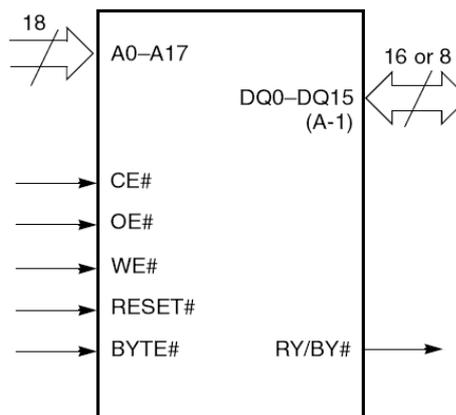
Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to Figure 9 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to "Word/Byte Configuration" for more information.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 2 and 3 indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

AMD

Am29F400B

4 Megabit (512 K x 8-Bit/256 K x 16-Bit)
CMOS 5.0 Volt-only Boot Sector Flash Memory

Table 1. Am29F400B Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	A0–A17	DQ0–DQ7	DQ8–DQ15 BYTE# = V_{IH}	DQ8–DQ15 BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	High-Z
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	High-Z
CMOS Standby	$V_{CC} \pm$ 0.5 V	X	X	$V_{CC} \pm$ 0.5 V	X	High-Z	High-Z	High-Z
TTL Standby	H	X	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect (See Note)	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	X

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In

Table 2. Am29F400BT Top Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal) (x8) Address Range	Address Range (in hexadecimal) (x16) Address Range
SA0	0	0	0	X	X	X	64/32	00000h–0FFFFh	00000h–07FFFh
SA1	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA2	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA3	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA4	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA5	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA6	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA7	1	1	1	0	X	X	32/16	70000h–77FFFh	38000h–3BFFFh
SA8	1	1	1	1	0	0	8/4	78000h–79FFFh	3C000h–3CFFFh
SA9	1	1	1	1	0	1	8/4	7A000h–7BFFFh	3D000h–3DFFFh
SA10	1	1	1	1	1	X	16/8	7C000h–7FFFFh	3E000h–3FFFFh

Table 3. Am29F400BB Bottom Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/Kwords)	Address Range (in hexadecimal) (x8) Address Range	Address Range (in hexadecimal) (x16) Address Range
SA0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh
SA1	0	0	0	0	1	0	8/4	04000h–05FFFh	02000h–02FFFh
SA2	0	0	0	0	1	1	8/4	06000h–07FFFh	03000h–03FFFh
SA3	0	0	0	1	X	X	32/16	08000h–0FFFFh	04000h–07FFFh
SA4	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA5	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA6	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA7	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA8	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA9	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA10	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh

Note:
Address range is A17:A-1 in byte mode and A17:A0 in word mode. See the "Word/Byte Configuration" section for more information.

3-Wire Serial EEPROMS	93Cx6

Description

The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to VCC and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operations are essential.

Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect

DI — **DO**
SK
CS — M93Cx6
ORG
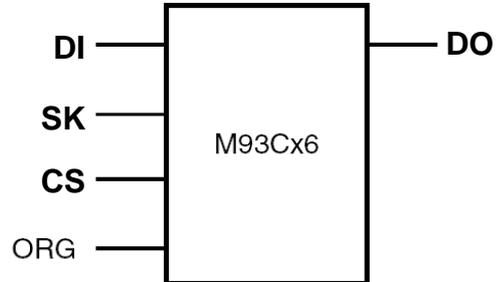
The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

Table 6.   **Instruction set for the M93C56 and M93C66**

Instruction	Description	Start bit	Op-code	x8 origination (ORG = 0)			x16 origination (ORG = 1)		
				Address (1) (2)	Data	Required clock cycles	Address (1) (3)	Data	Required clock cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0		A7-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
ERASE	Erase Byte or Word	1	11	A8-A0		12	A7-A0		11

1.   X = Don't Care bit.   2.   Address bit A8 is not decoded by the M93C56.   3.   Address bit A7 is not decoded by the M93C56.

Read Data

The Read Data from Memory (READ) instruction outputs data on Serial Data Output (Q).

When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 8-bit byte or 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Cx6 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input (S) is held High. In this case, the dummy 0 bit is *not* output between bytes (or words) and a continuous stream of data can be read.

Write Data

For the Write Data to Memory (WRITE) instruction, 8 or 16 data bits follow the op-code and address bits. These form the byte or word that is to be written. As with the other bits, Serial Data Input (D) is sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken low before the next rising edge of Serial Clock (C).* If Chip Select Input (S) is brought low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described later in this document.

Once the Write cycle has been started, it is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle). The cycle is automatically preceded by an Erase cycle, so it is unnecessary to execute an explicit erase instruction before a Write Data to Memory (WRITE) instruction.

3-Wire Serial EEPROMS	**93Cx6**

Synchronous Data Timing
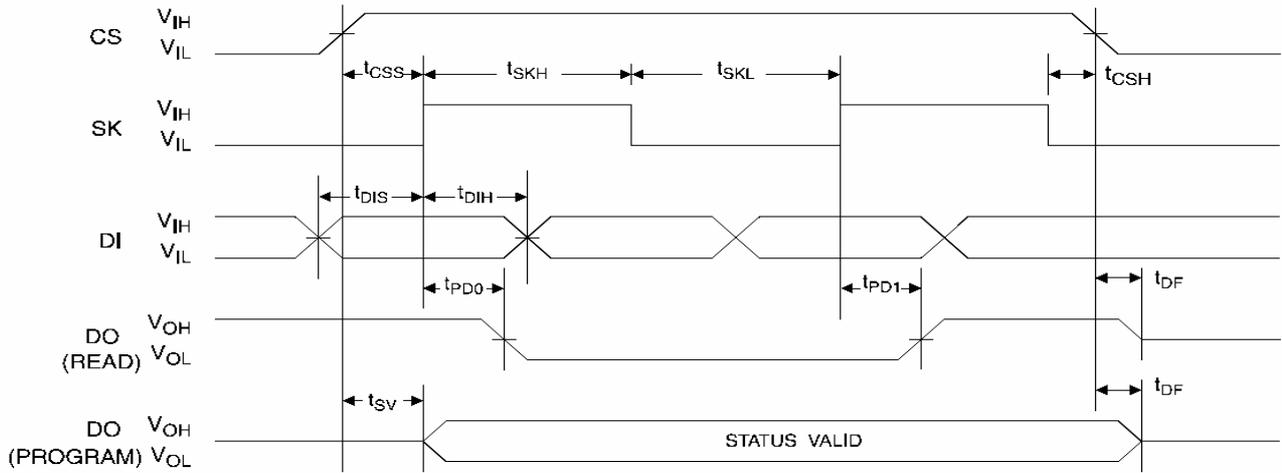
WRITE Timing
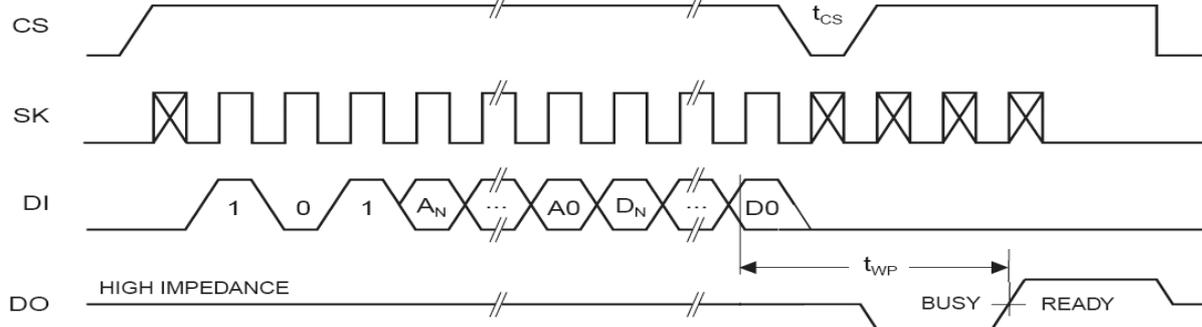
READ Timing
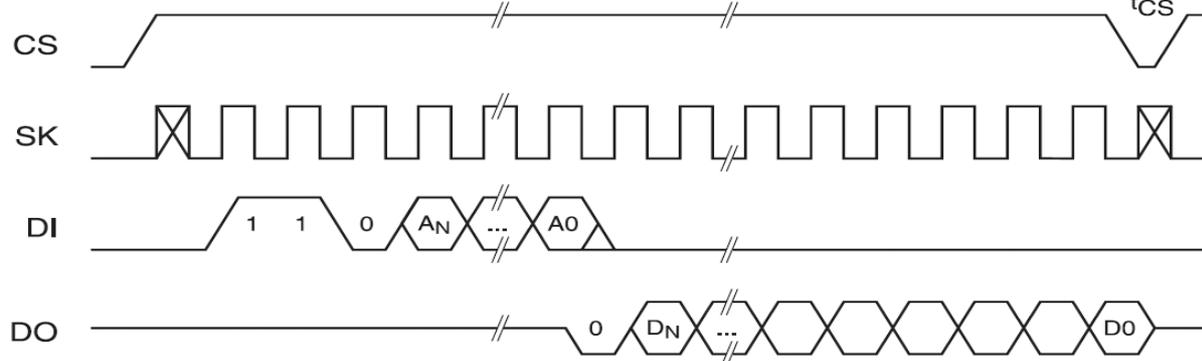
The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally–controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs				ON Switches				
Inhibit	C*	B	A	MC14051B	MC14052B		MC14053B		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

* Not applicable for MC14052
x = Don't Care
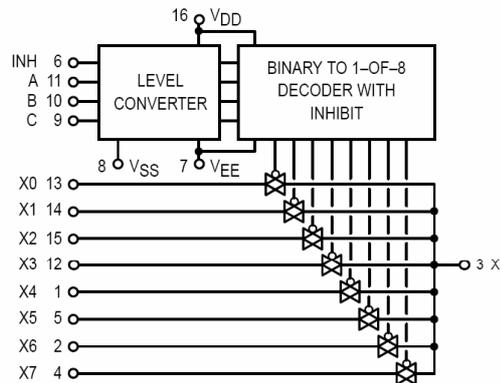
**Figure 2. MC14051B Functional Diagram**
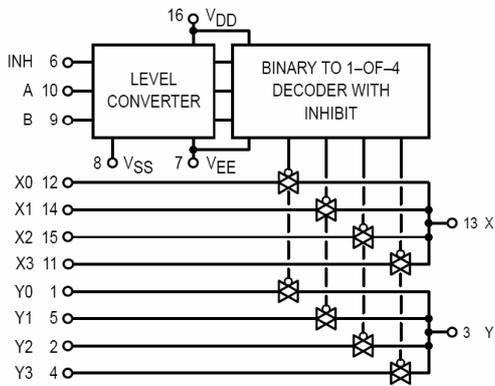

Figure 3. MC14052B Functional Diagram
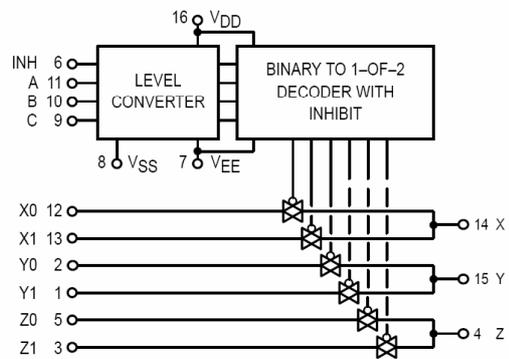
Figure 4. MC14053B Functional Diagram

| 74HC151	74HC138
74HC151 8 Channel Digital Multiplexer	**74HC138** 3 to 8 Line Decoder

| Description	
Description This high speed Digital multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HC151/MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.	The M54/74HC138 is a high speed CMOS 3 TO 8 LINE DECODER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of the outputs will go low. If enable input G1 is held low or either G2A or G2B is held high, the decoding function is inhibited and all the 8 outputs go high. Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems.

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input
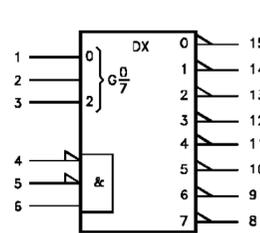
PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$, $\overline{G2B}$	Enable Inputs
6	G1	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y0}$ to $\overline{Y7}$	Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G2B	G2A	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X: Don't Care

FAIRCHILD
SEMICONDUCTOR ™

QFET®

FQB19N20L / FQI19N20L

## 200V LOGIC N-Channel MOSFET

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supply, motor control.

Features

- 21A, 200V, $R_{DS(on)} = 0.14\Omega$ @$V_{GS} = 10$ V
- Low gate charge (typical 27 nC)
- Low Crss (typical 30 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Low level gate drive requirement allowing direct operation from logic drivers
- RoHS Compliant

100% LEAD-FREE IMPLEMENTATION

D

G S **D²-PAK**
FQB Series

G D S **I²-PAK**
FQI Series

D
G
S
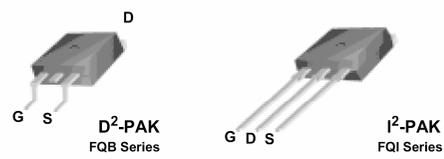
Absolute Maximum Ratings $T_C = 25°C$ unless otherwise noted

Symbol	Parameter			FQB19N20L / FQI19N20L	Units
V_{DSS}	Drain-Source Voltage			200	V
I_D	Drain Current	- Continuous ($T_C = 25°C$)		21	A
		- Continuous ($T_C = 100°C$)		13.3	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	84	A
V_{GSS}	Gate-Source Voltage			± 20	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	250	mJ
I_{AR}	Avalanche Current		(Note 1)	21	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	14	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25°C$) *			3.13	W
	Power Dissipation ($T_C = 25°C$)			140	W
		- Derate above 25°C		1.12	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.89	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

a

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	200	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C	--	0.16	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200$ V, $V_{GS} = 0$ V	--	--	1	µA
		$V_{DS} = 160$ V, $T_C = 125°C$	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 10.5$ A	--	0.11	0.14	Ω
		$V_{GS} = 5$ V, $I_D = 10.5$ A (Note 4)		0.12	0.15	
g_{FS}	Forward Transconductance	$V_{DS} = 30$ V, $I_D = 10.5$ A	--	18.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	1700	2200	pF
C_{oss}	Output Capacitance		--	220	290	pF
C_{rss}	Reverse Transfer Capacitance		--	30	40	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100$ V, $I_D = 21$ A, $R_G = 25$ Ω (Note 4, 5)	--	35	80	ns
t_r	Turn-On Rise Time		--	300	610	ns
$t_{d(off)}$	Turn-Off Delay Time		--	130	270	ns
t_f	Turn-Off Fall Time		--	180	370	ns
Q_g	Total Gate Charge	$V_{DS} = 160$ V, $I_D = 21$ A, $V_{GS} = 5$ V (Note 4, 5)	--	27	35	nC
Q_{gs}	Gate-Source Charge		--	5.8	--	nC
Q_{gd}	Gate-Drain Charge		--	11.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	21	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	84	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 21$ A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 21$ A (Note 4)	--	140	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F / dt = 100 A/µs	--	0.66	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 0.85mH, I_{AS} = 21A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 21A, di/dt $\leq$ 300A/µs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300µs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature

10.6 10-BIT A/D CONVERTER (ADC)

10.6.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

10.6.2 Main Features

10-bit conversion
Up to 16 channels with multiplexed input
Linear successive approximation
Data register (DR) which contains the results
Conversion complete status flag
On/off bit (to reduce consumption)

10.6.3 Functional Description

The conversion is monotonic, meaning that the result never decreases if the analog input does not and never increases if the analog input does not.

If the input voltage (VAIN) is greater than VAREF (high-level voltage reference) then the conversion result is FFh in the ADCDRH register and 03h in the ADCDRL register (without overflow indication).

If the input voltage (VAIN) is lower than VSSA (lowlevel voltage reference) then the conversion result in the ADCDRH and ADCDRL registers is 00 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDRH and ADCDRL registers. The accuracy of the conversion is described in the Electrical Characteristics Section.

RAIN is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the allowed time.

10.6.3.1 A/D Converter Configuration

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the «I/O ports» chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the ADCCSR register:
– Select the CS[3:0] bits to assign the analog channel to convert.

10.6.3.2 Starting the Conversion

In the ADCCSR register:
– Set the ADON bit to enable the A/D converter and to start the conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete:
To read the 10 bits, perform the following steps:
1. Poll the EOC bit
2. Read the ADCDRL register
3. Read the ADCDRH register. This clears EOC automatically.

10.6.6 Register Description

CONTROL/STATUS REGISTER (ADCCSR)

Read/Write (Except bit 7 read only)

Reset Value: 0000 0000 (00h)

Bit 7 = **EOC** End of Conversion

This bit is set by hardware. It is cleared by hardware when software reads the ADCDRH register or writes to any bit of the ADCCSR register.

0: Conversion is not complete

1: Conversion complete

Bit 6 = **SPEED** ADC clock selection

This bit is set and cleared by software.

0: fADC = fCPU/4

1: fADC = fCPU/2

Bit 5 = **ADON** A/D Converter on

This bit is set and cleared by software.

0: Disable ADC and stop conversion

1: Enable ADC and start conversion

Bit 4 = **Reserved.** Must be kept cleared.

Bit 3:0 = **CH[3:0]** Channel Selection

These bits are set and cleared by software. They select the analog input to convert.

Channel Pin	CH3	CH2	CH1	CH0
AIN0	0	0	0	0
AIN1	0	0	0	1
AIN2	0	0	1	0
AIN3	0	0	1	1
AIN4	0	1	0	0
AIN5	0	1	0	1
AIN6	0	1	1	0
AIN7	0	1	1	1
AIN8	1	0	0	0
AIN9	1	0	0	1
AIN10	1	0	1	0
AIN11	1	0	1	1
AIN12	1	1	0	0
AIN13	1	1	0	1
AIN14	1	1	1	0
AIN15	1	1	1	1

DATA REGISTER (ADCDRH)

Read Only

Bit 7:0 = **D[9:2]** MSB of Converted Analog Value

DATA REGISTER (ADCDRL)

Read Only

Bit 1:0 = **D[1:0]** LSB of Converted Analog Value

Table 22. ADC Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0070h	**ADCCSR** Reset Value	EOC 0	SPEED 0	ADON 0	0	CH3 0	CH2 0	CH1 0	CH0 0
0071h	**ADCDRH** Reset Value	D9 0	D8 0	D7 0	D6 0	D5 0	D4 0	D3 0	D2 0
0072h	**ADCDRL** Reset Value	0	0	0	0	0	0	D1 0	D0 0

| LOW POWER QUAD VOLTAGE COMPARATOR	**LM2901**

DESCRIPTION

The LM2901 consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common–mode voltage range includes ground, even though they are operated from a single power supply voltage.

The LM2901 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM2901 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

EQUIVALENT CIRCUIT
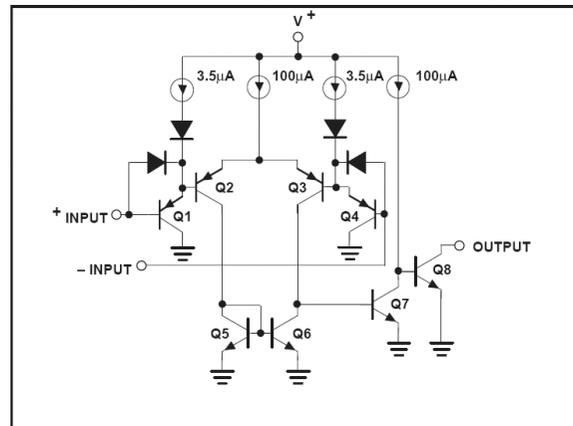
DC AND AC ELECTRICAL CHARACTERISTICS

V+=5V_{DC}, LM2901: –40°C ≤ T_A ≤ 125°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LM2901			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	T_A=25°C		±2.0	±7.0	mV
		Over temp.		±9	±15	mV
V_{CM}	Input common–mode voltage range	T_A=25°C	0		V+−1.5	V
		Over temp.	0		V+−2.0	
V_{IDR}	Differential input voltage	Keep all V_{IN}^{s}≥0V_{DC} (or V− if need)			V+	V
I_{BIAS}	Input bias current	$I_{IN(+)}$ or $I_{IN(−)}$ with output in linear range				
		T_A=25°C		25	250	nA
		Over temp.		200	500	nA
I_{OS}	Input offset current	$I_{IN(+)}$−$I_{IN(−)}$				
		T_A=25°C		±5	±50	nA
		Over temp.		±50	±200	nA
I_{OL}	Output sink current	$V_{IN(−)}$≥1V_{DC}, $V_{IN(+)}$=0, V_O≤1.5V_{DC}, T_A=25°C	6.0	16		mA
	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN(−)}$=0 V_O=5V_{DC}, T_A=25°C		0.1		nA
I_{CC}	Supply current	R_L=∞ on all comparators,				mA
		T_A=25°C		0.8	2.0	
		R_L=∞ on all comparators, V+=30V		1.0	2.5	mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(−)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C			400	mV
		Over temp.		400	700	mV
t_{LSR}	Large–signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		300		ns
t_R	Response time	V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		1.3		µs

TLE6250G

Description

The CAN-transceiver TLE 6250 is a monolithic integrated circuit. The IC is optimized for high speed differential mode data transmission in automotive and industrial applications. It works as an interface between the CAN protocol controller and the physical differential bus in both, 12 V and 24 V systems.
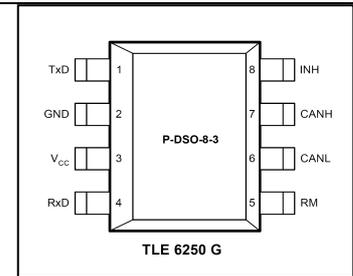
Pin No. Symbol Function

1. TxD **CAN transmit data input;** 20 kΩpull up, LOW in dominant state
2. GND **Ground;**
3. VCC **5 V Supply;**
4. RxD **CAN receive data output;** LOW in dominant state, integrated pull up
5. RM **Receive-only input;** (5 V-version), 20 kΩpull up, set low to activate RxD-only mode
6. CANL **Low line input;** LOW in dominant state
7. CANH **High line output;** HIGH in dominant state
8. INH **Control input;** 20 kΩpull, set LOW for normal mode

Functional Block Diagram
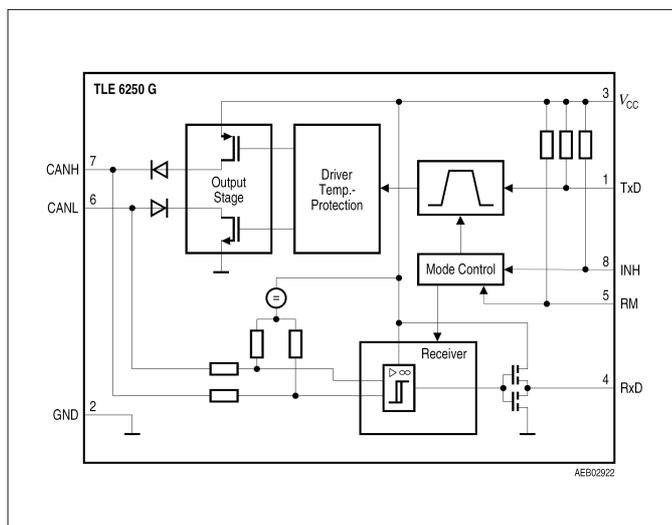
Figure 2   Block Diagram TLE 6250 G
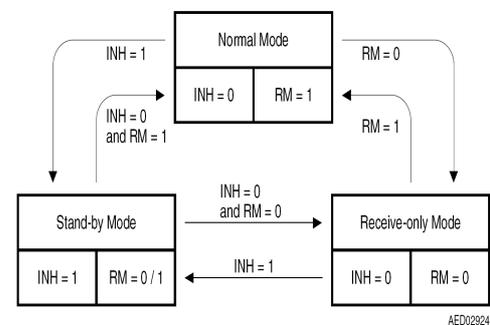
5V Version

Functional Description

The TLE 7209-2R is an intelligent full H-Bridge, designed for the control of DC and stepper motors in safety critical applications and under extreme environmental conditions.

Table 1   Pin Definitions and Functions

Pin. No.	Symbol	Function
1	GND	Ground
2	SCK/SF	SPI-Clock/Status-flag
3	IN1	Input 1
4	V_SCP	Supply voltage for internal charge pump
5, 16	V_S	Supply voltage; connect pins externally
6, 7	OUT1	Output 1; connect pins externally
8	SDO	Serial data out
9	SDI	Serial data in
10	GND	Ground
11	GND	Ground

Overv

Table 1   Pin Definitions and Functions (cont'd)

Pin. No.	Symbol	Function
12	DMS	Diagnostic-Mode selection (+ Supply voltage for SPI-Interface)
13	EN	Enable
14, 15	OUT2	Output 2; connect pins externally
17	CSN	Chip Select (low active)
18	DIS	Disable
19	IN2	Input 2
20	GND	Ground

Table 2   Functional Truth Table

Pos.	DIS	EN	IN1	IN2	OUT1	OUT2	SF[1]	SPI[2] DIA_REG
1. Forward	L	H	H	L	H	L	H	see Chapter 2.4.2
2. Reverse	L	H	L	H	L	H	H	
3. Free-wheeling low	L	H	L	L	L	L	H	
4. Free-wheeling high	L	H	H	H	H	H	H	
5. Disable	H	X	X	X	Z	Z	L	
6. Enable	X	L	X	X	Z	Z	L	
7. IN1 disconnected	L	H	Z	X	H	X	H	
8. IN2 disconnected	L	H	X	Z	X	H	H	
9. DIS disconnected	Z	X	X	X	Z	Z	L	
10. EN disconnected	X	Z	X	X	Z	Z	L	
11. Current limit. active	L	H	X	X	Z	Z	H	
12. Under Voltage	X	X	X	X	Z	Z	L	
13. Over-temperature	X	X	X	X	Z	Z	L	
14. Over-current	X	X	X	X	Z	Z	L	

[1] If Mode "Status-Flag" is selected (see **Chapter 2.4**)

[2] If Mode "SPI-Diagnosis" is selected (see **Chapter 2.4**)
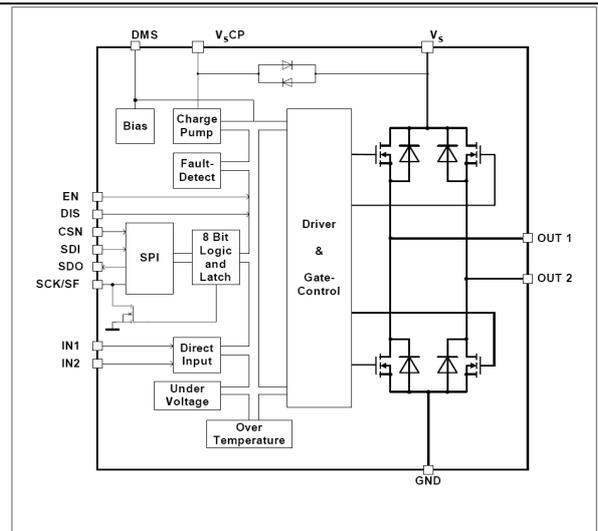
Figure 2   Block Diagram TLE 7209-2R

DOCUMENTATION Bus CAN

Exemple de configuration de bus CAN automobile.
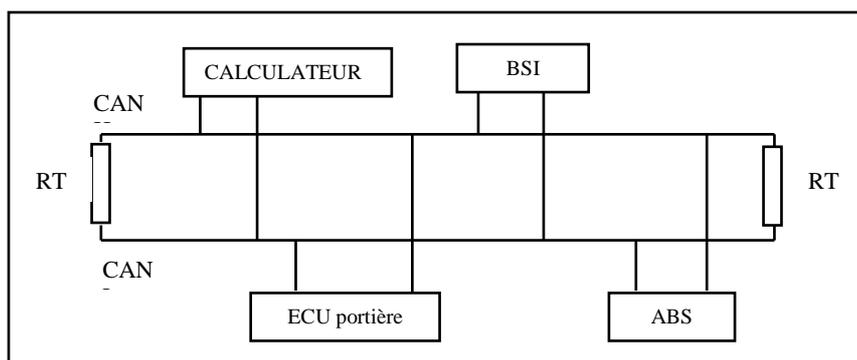
Le bus CAN est composé de 2 fils (torsadés) et de 2 résistances de terminaison RT de 120 Ω environ (permet d'éviter le phénomène de réflexion). Le principe de fonctionnement est simple, les signaux sont complémentaires mais les 0 et 1 logiques ne sont pas situés aux même tensions pour CAN-H et CAN-L. En réalisant la soustraction des 2 signaux, on recompose le signal de départ.

C'est un bus série de type multi - maître, c'est-à-dire que toutes les stations reliées au bus peuvent émettre un message lorsque le bus est libre. Le message contient un identificateur qui permet d'en définir la priorité. Le message de plus haute priorité prendra possession du bus.

Toutes les stations recevront le message, mais seule celle concernée (reconnue grâce à l'identificateur) le traite.

Le débit varie de 125kbits/s à 1 Mbit/s pour le protocole HS (« High Speed »).

Le couplage physique au réseau est fait sur le principe du « OU câblé », c'est-à-dire qu'un niveau bas écrase un niveau haut en cas d'émission simultanée. On ne parlera donc pas d'état logique 0 et 1, mais d'états dominants et récessifs. L'état 0 correspond à un état dominant et l'état 1 à un état récessif.

Trois types de trame peuvent circuler sur le bus : trame de requête, trame de données et trame d'erreur.

La norme 2.0B définit deux formats de protocole, la version standard et étendue. La version étendue permet d'avoir un plus grand nombre de stations sur le réseau, le nombre maximum d'octets de données est inchangé. Les deux formats sont compatibles et peuvent se trouver sur un même réseau.

Une trame de données au format 2.0B est constituée selon un des modèles ci-dessous.
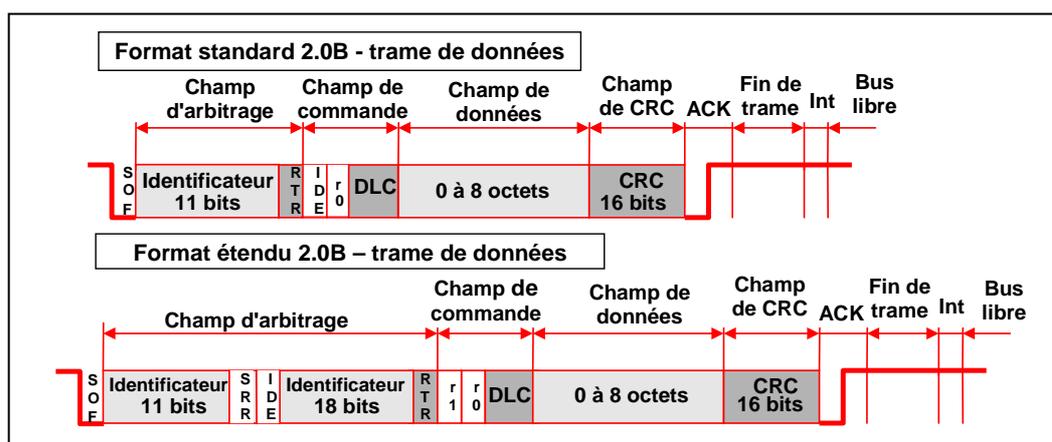
Début de trame : SOF

Constitué par un seul bit de niveau dominant qui indique aux stations le début du dialogue. Celles-ci doivent se synchroniser sur le front de la transition.

Champ d'arbitrage

Constitué des bits de l'identificateur et des bits RTR (« Remote Transmission Request bit »), plus les bits SRR (« Subtitute Remote Request bit ») et IDE (« Identifier Extension bit ») pour le format étendu.

L'identificateur est de 11 bits pour un format standard et de 29 bits pour un format étendu (le bit MSb étant transmis en tête).

Le bit RTR indique une requête de transmission à distance, il est au niveau dominant pour une trame de donnée et au niveau récessif pour une trame de requête.

Le bit SRR est à l'état récessif pour les trames de données et de requêtes.

Le bit IDE ne se trouve dans le champ d'arbitrage que pour une trame au format étendu, il est alors au niveau récessif.

Le champ d'arbitrage permet de reconnaître la priorité du message. En cas d'émission simultanée, le premier message qui aura un bit dominant (alors que l'autre a un bit récessif) prendra la priorité sur la ligne.

Champ de commande

Constitué de 6 bits :
- Le bit IDE ne se trouve dans le champ de commande que pour une trame au format standard, il est alors au niveau dominant.
- Les bits r1 (format étendu uniquement) et r0 sont réservés pour une évolution future du protocole. Ils sont toujours au niveau dominant.
- Ensuite les 4 autres bits forment le champ DLC et indiquent le nombre d'octets qui seront transmis dans le champ de données.

Champ de données : DATA

Constitué de 0 à 8 octets de données utiles (MSb est transmis en tête).

Champ CRC :

Constitué de 15 bits suivi d'un délimiteur au niveau récessif. C'est un code de contrôle qui est transmis.

Champ d'acquittement : ACK

Constitué de 2 bits « ACK Slot » au niveau dominant et « Delimiter » au niveau récessif.

Fin de trame : EOF.

Constitué de 7 bits au niveau récessif. Il permet d'identifier la fin de la trame.

Technique de « Bit Stuffing » :

Pour éviter d'avoir une succession trop importante de bits dans le même état, et ceci pour améliorer la synchronisation, on insère un bit d'un état opposé dès que l'on a transmis cinq bits identiques à la suite.
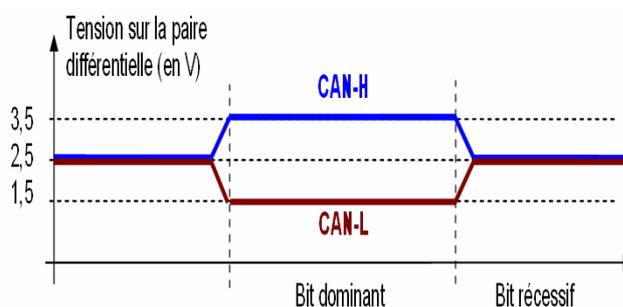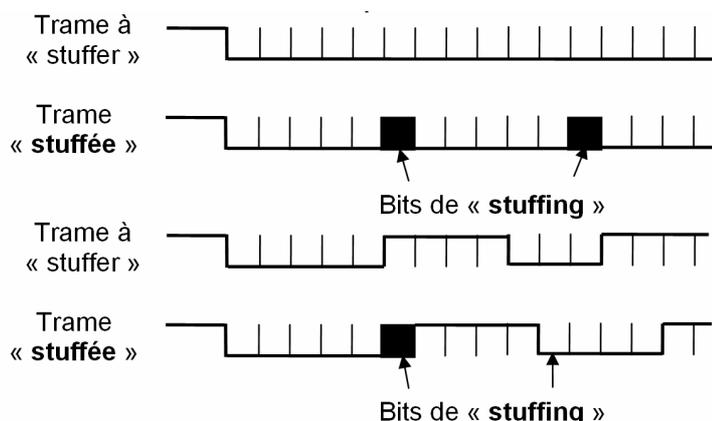
Caractéristiques électriques pour une transmission de type HS

La transmission de données est effectuée sur une paire filaire différentielle. Elle est constituée de deux fils : CAN-L et CAN-H. (Note: 2.5V < CAN-H < 3.5V   et 1.5V < CAN-L < 2.5V)

OCTAL D TYPE FLIP FLOP WITH CLEAR	74HC274

The M54/74HC273 is a high speed CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated in silicon gate C2 MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.

When the CLEAR input is held low, the Q output are in the low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN DESCRIPTION

SYMBOL	NAME AND FUNCTION
CLEAR	Master Reset Input (Active LOW)
Q0 to Q7	Flip Flop Outputs
D0 to D7	Data Inputs
CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
GND	Ground (0V)
V_{CC}	Positive Supply Voltage

LOGIC DIAGRAM