FIGURES

Tournez la page S.V.P.

Figure 1 : tapis incliné

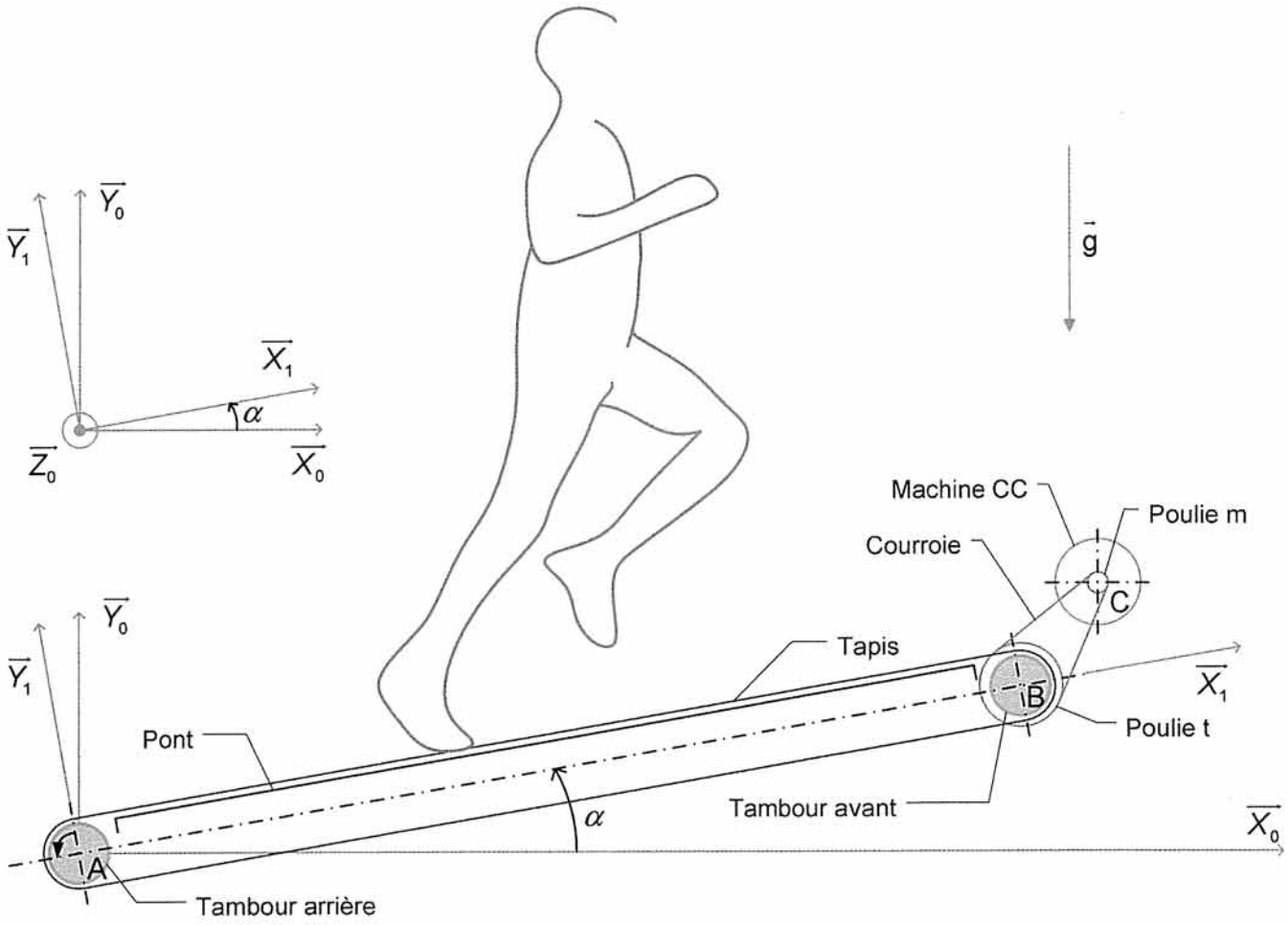


Figure 2 : tapis horizontal

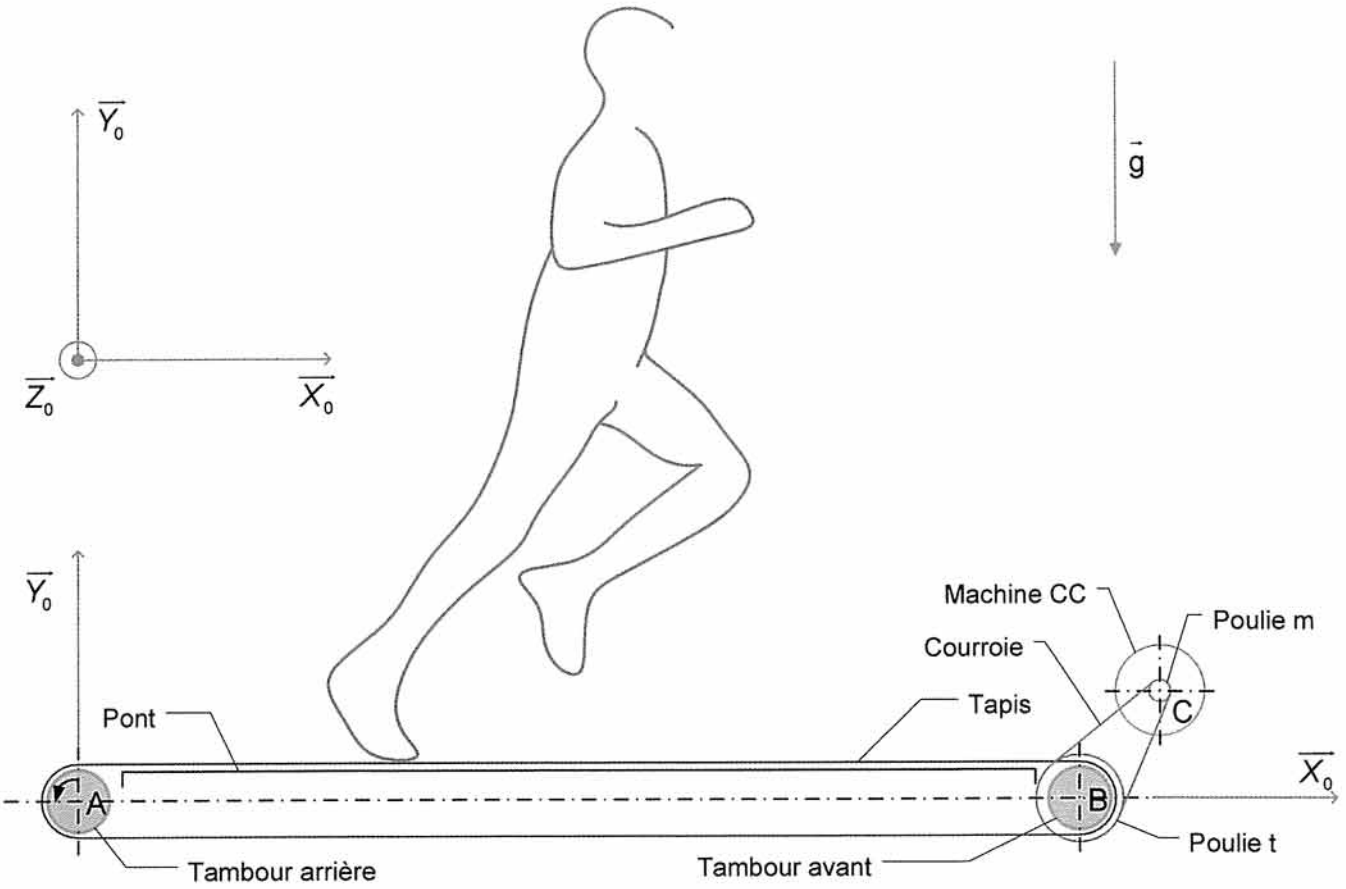
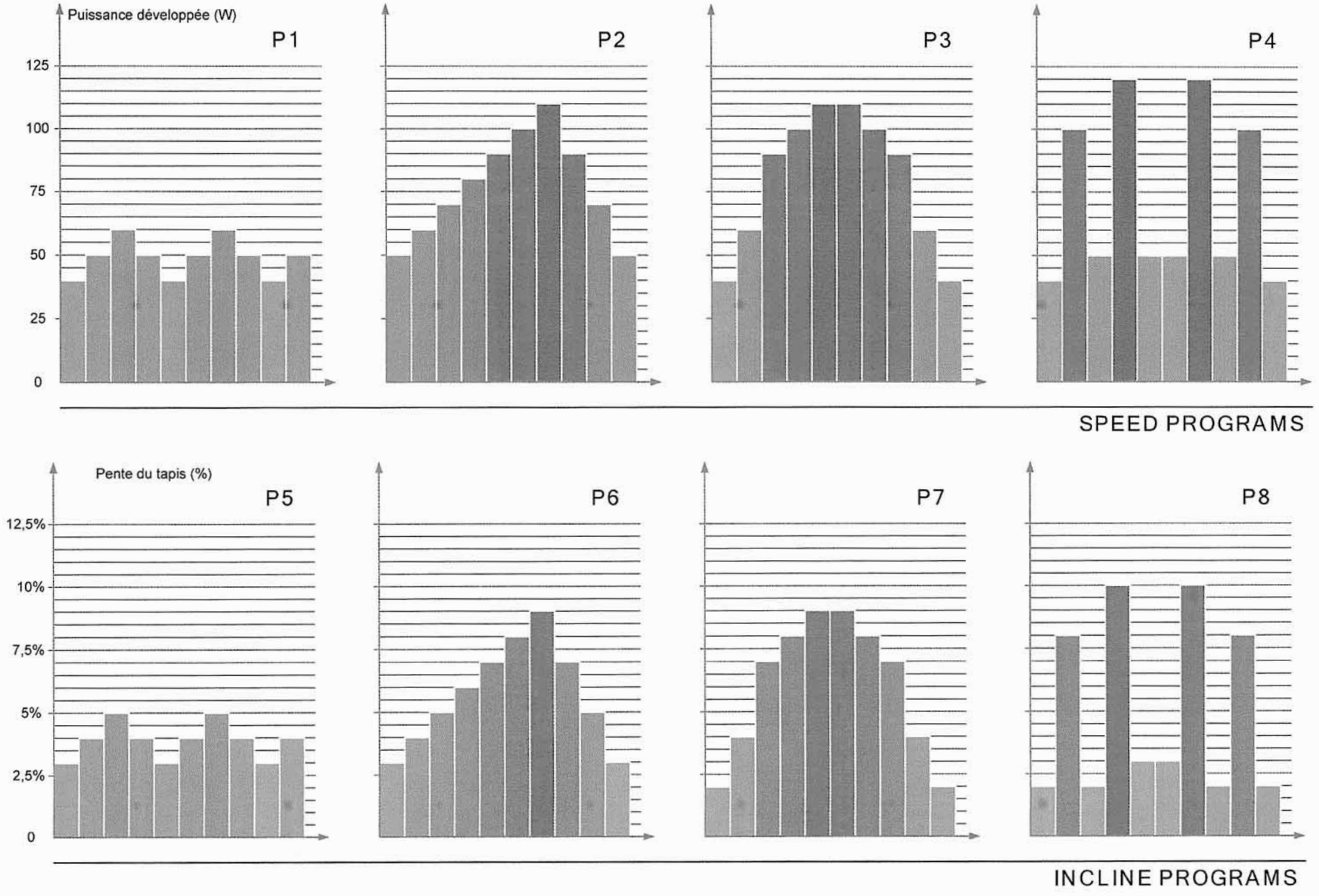
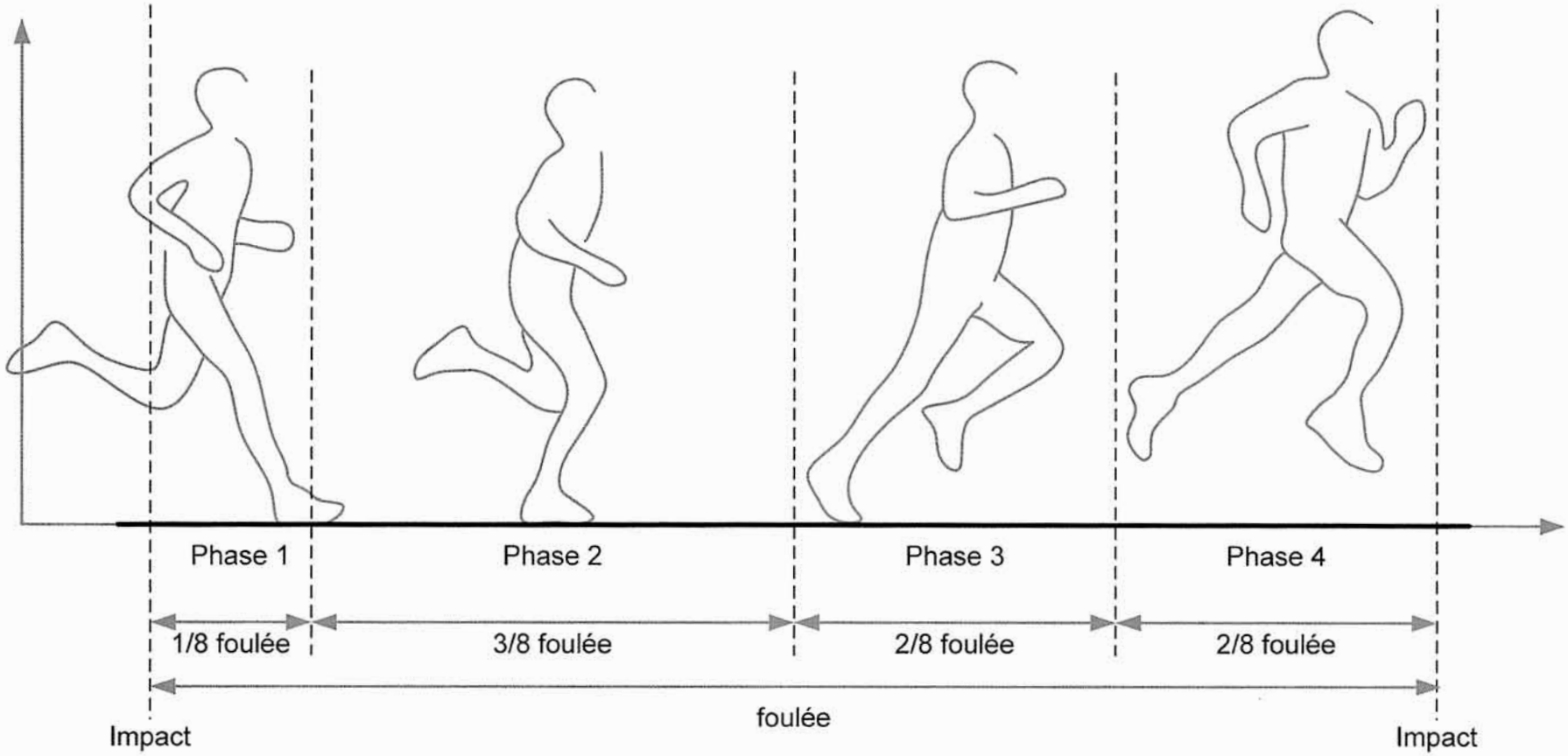


Figure 3 : cycles préprogrammés



Tournez la page S.V.P.

Figure 4 : description d'une foulée



L'impact définit l'instant où le coureur entre en contact avec le tapis du pied gauche ou du pied droit, la foulée la distance entre deux impacts successifs.

Phase 1 : phase d'amortissement.

Phase 2 : phase de maintien et de prise de vitesse.

Phase 3 : phase d'impulsion.

Phase 4 : phase de suspension.

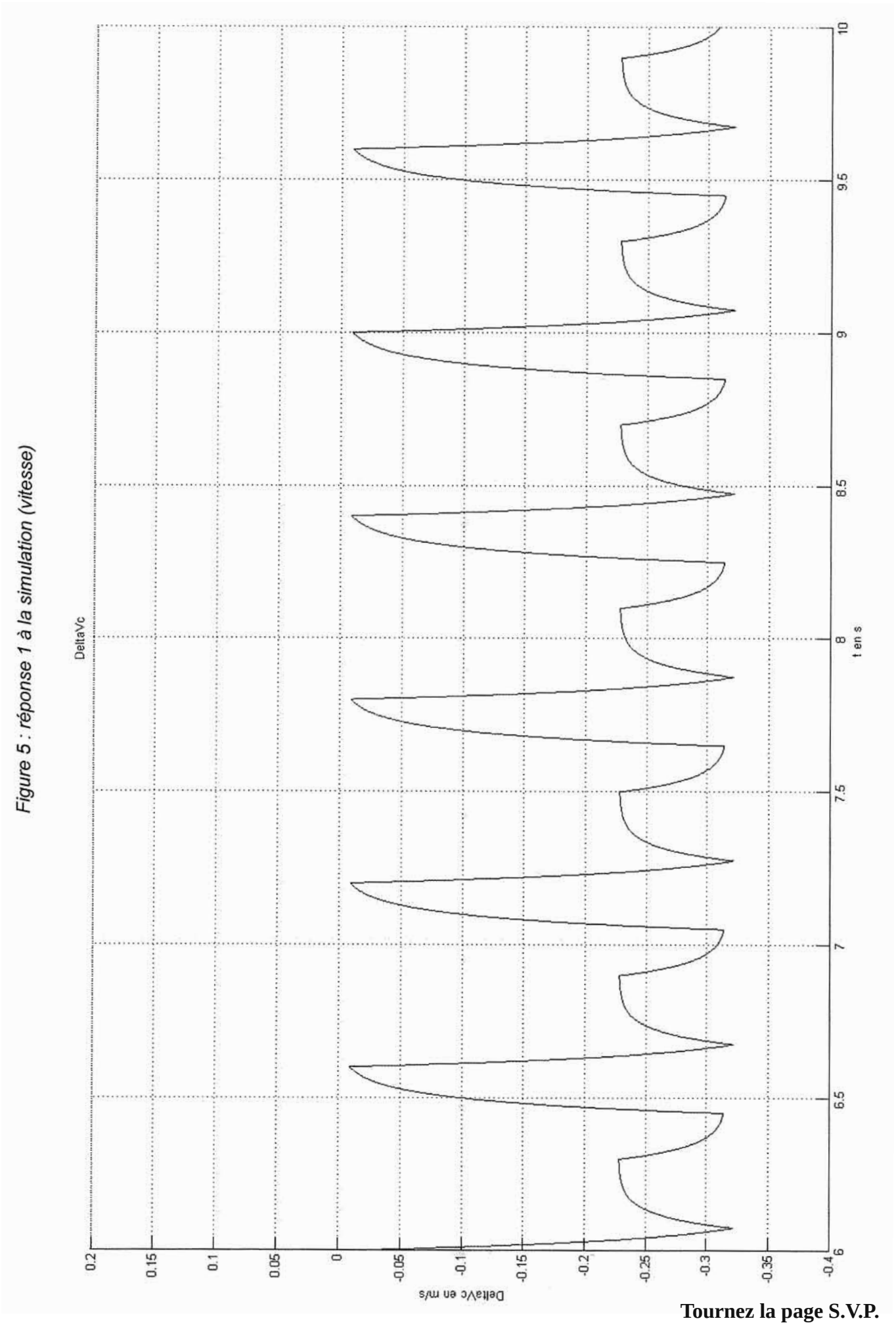
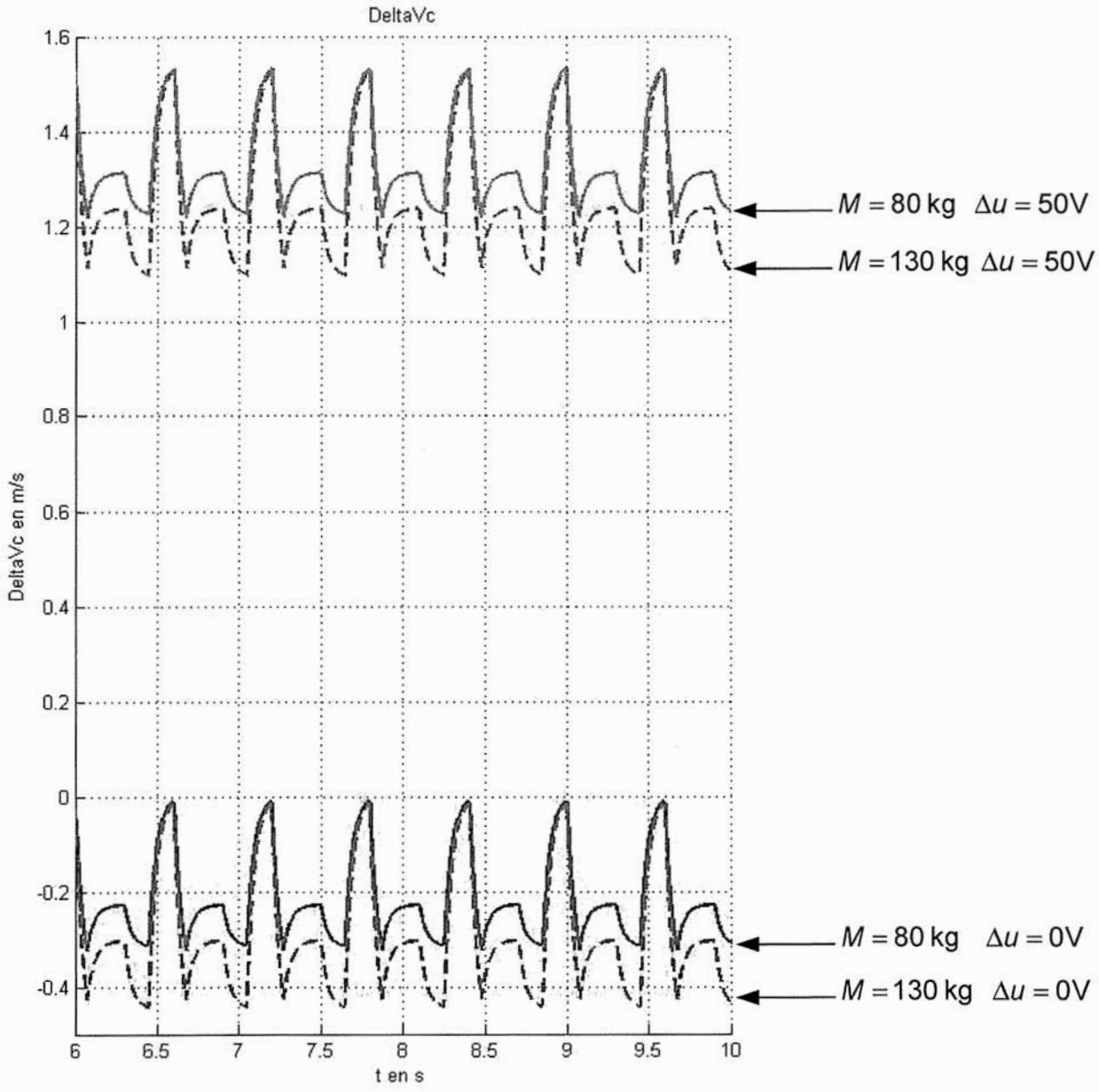


Figure 5 : réponse 1 à la simulation (vitesse)

Tournez la page S.V.P.

Figure 6 : réponse 2 à la simulation (vitesse)



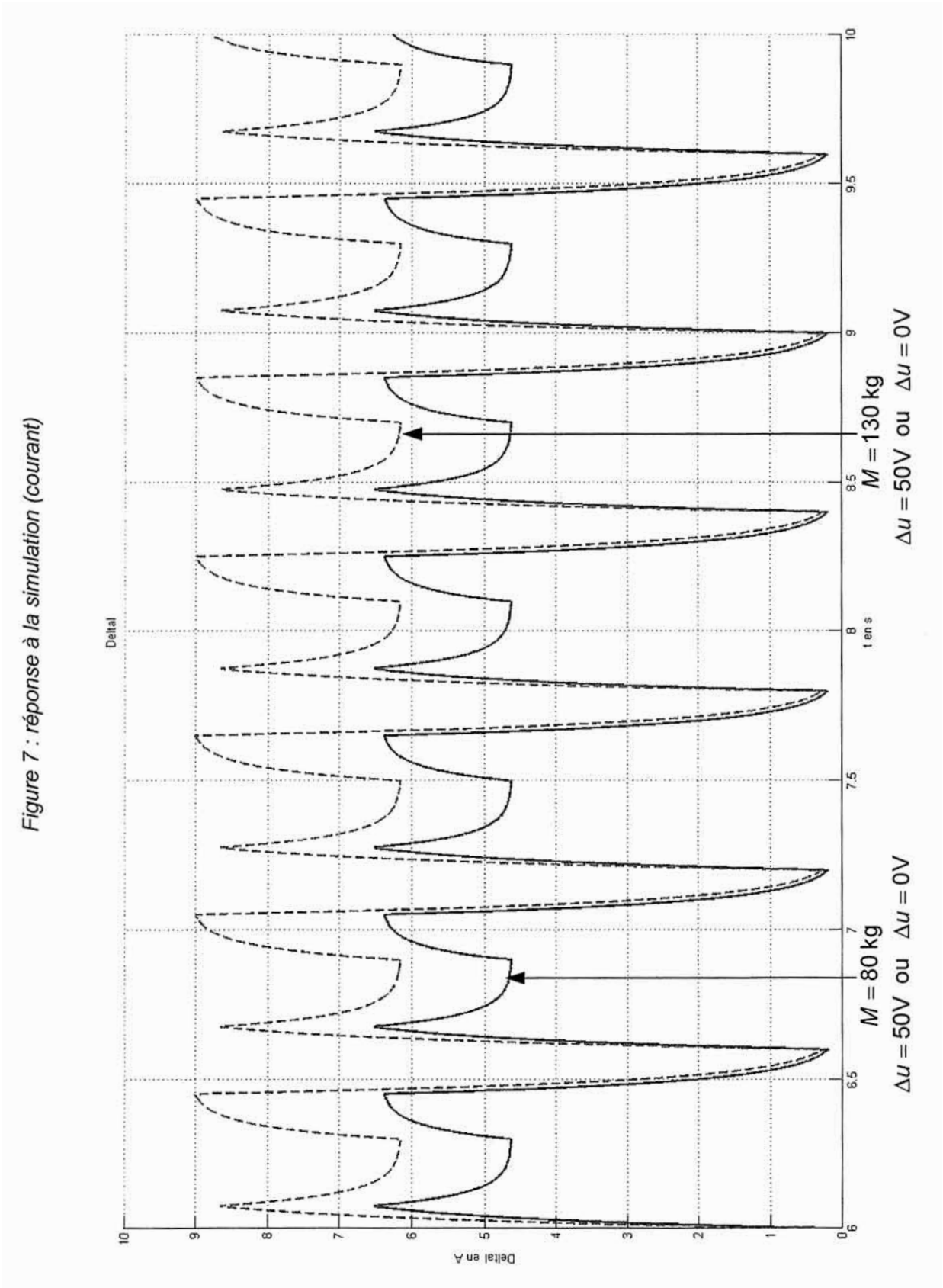


Figure 7 : réponse à la simulation (courant)

Tournez la page S.V.P.

Figure 8 : dispositif d'inclinaison du tapis

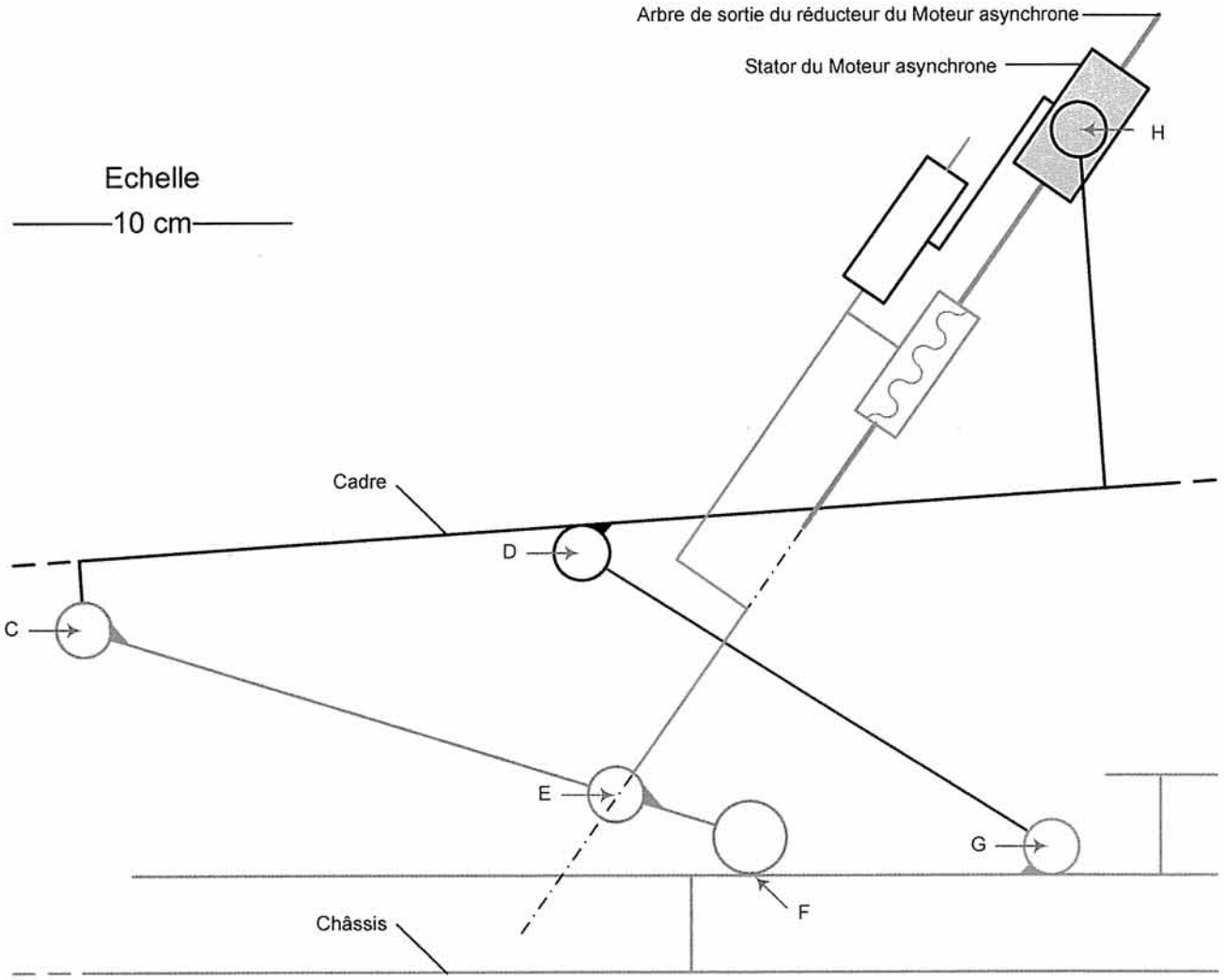
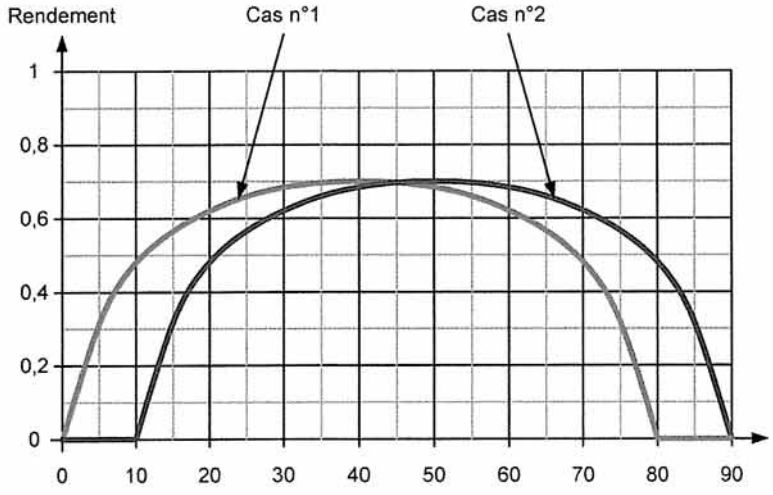


Figure 9 : rendement du dispositif vis-écrou

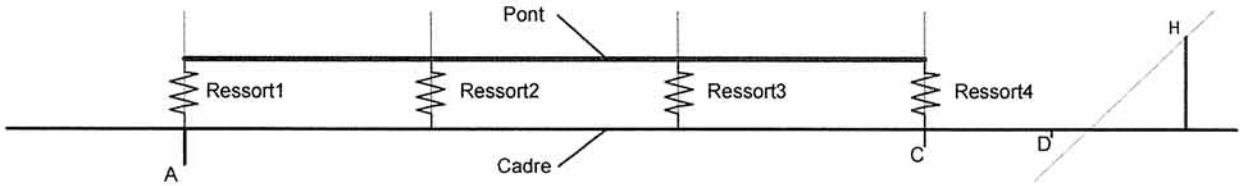


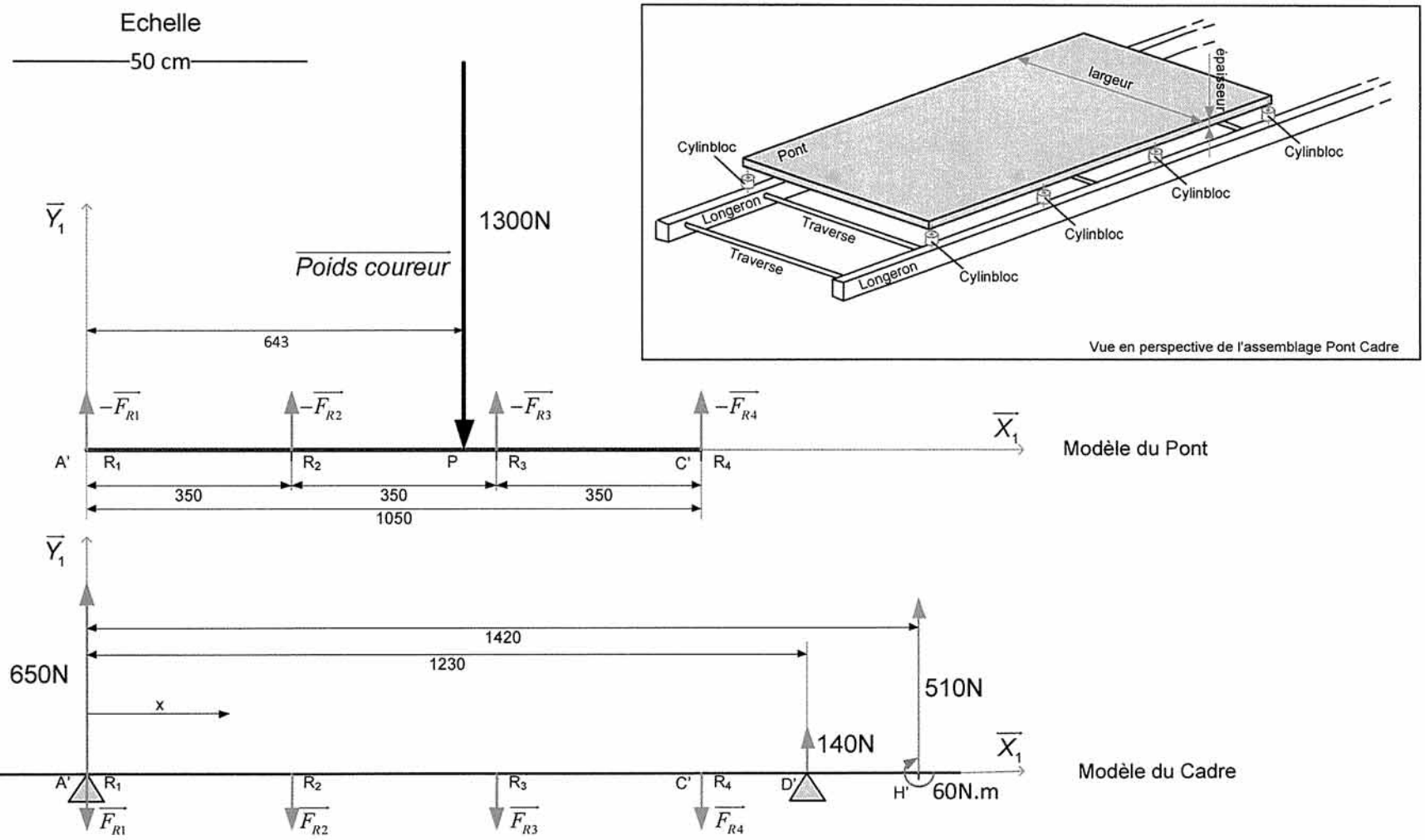
Le rendement d'un dispositif de transformation de mouvement est donné par le rapport (en valeur absolue) entre la puissance de sortie du mécanisme et sa puissance d'entrée.

Cas de sollicitation n°1: un couple moteur est appliqué à la vis et une charge résistante est imposée à l'écrou.

Cas de sollicitation n°2: une charge motrice est appliquée à l'écrou et un couple résistant est appliqué à la vis.

Figure 10 : modèles poutre du cadre et du pont





Tournez la page S.V.P.

Figure 11 : déformées du pont et du cadre

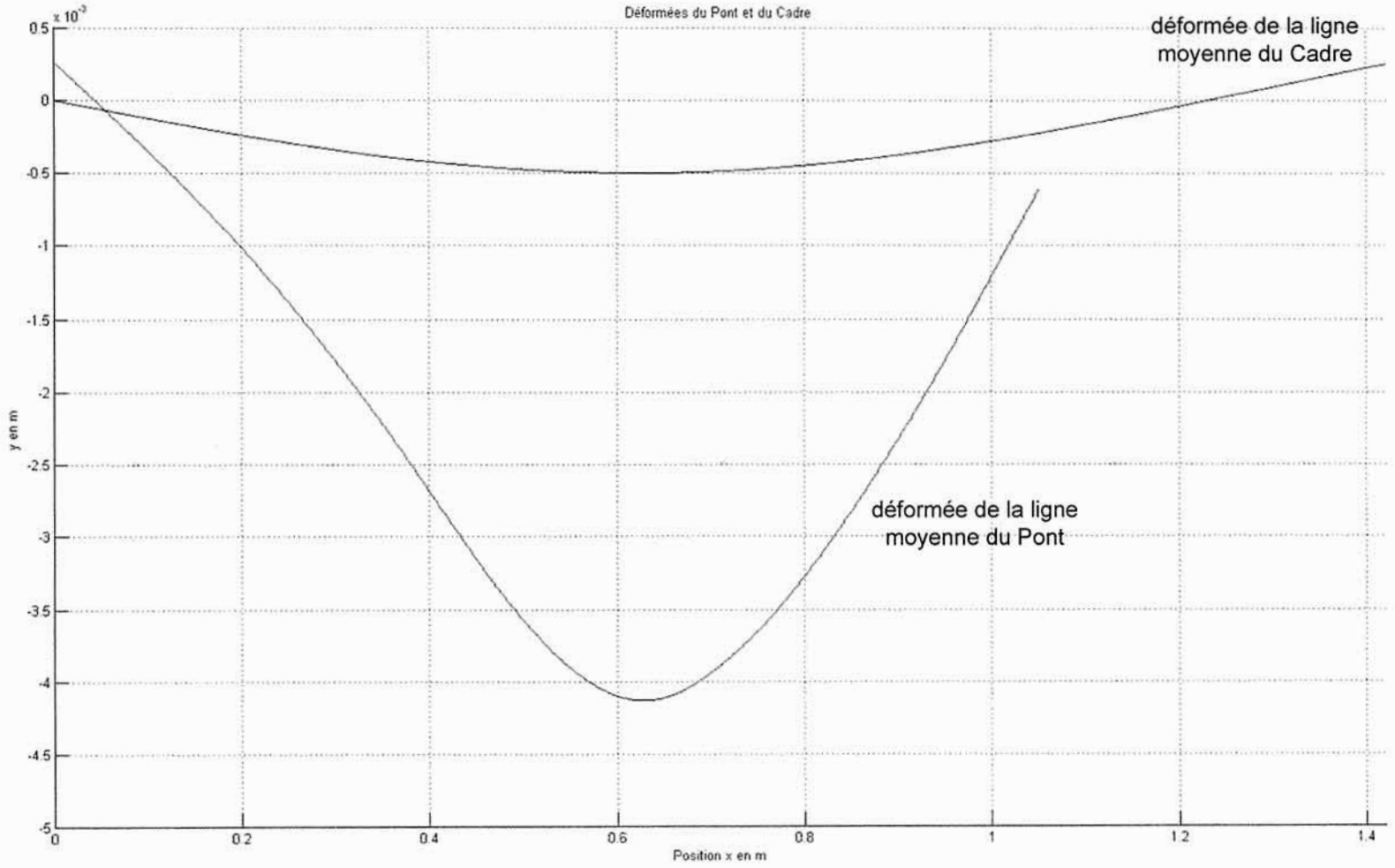


Figure 12 : distance EH en fonction de la pente du tapis

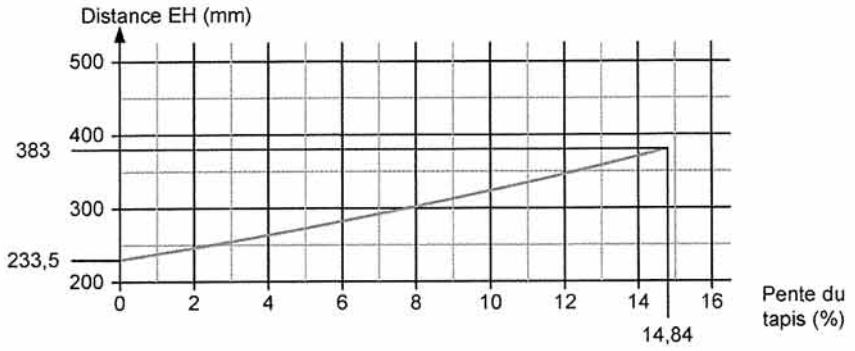
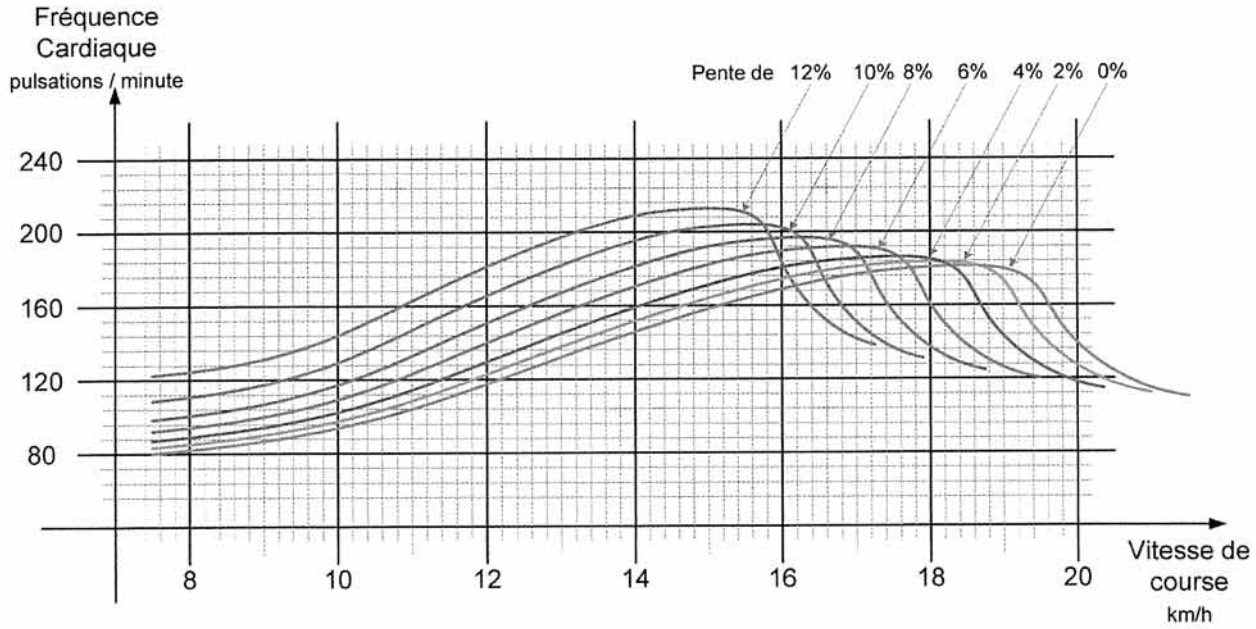
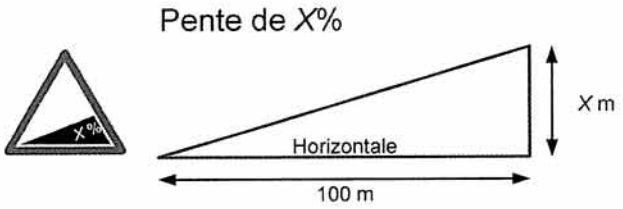


Figure 13 : réseau de courbes de fréquence cardiaque



Chaque courbe possède un maximum puisque, au-delà d'une certaine vitesse, le coureur rentre dans une phase de course en apnée (totale ou partielle). Cette phase ne peut être maintenue que temporairement.

Ce réseau de courbes est propre à chaque utilisateur.



DOCUMENTS RESSOURCE

Document Ressource 1 : microcontrôleur

Document Ressource 2 : diode électroluminescente orange

Document Ressource 3 : optocoupleur

Document Ressource 4 : résistances

Document Ressource 5 : afficheur

7.0 TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time-base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable, and is cleared on any device RESET.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4, or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

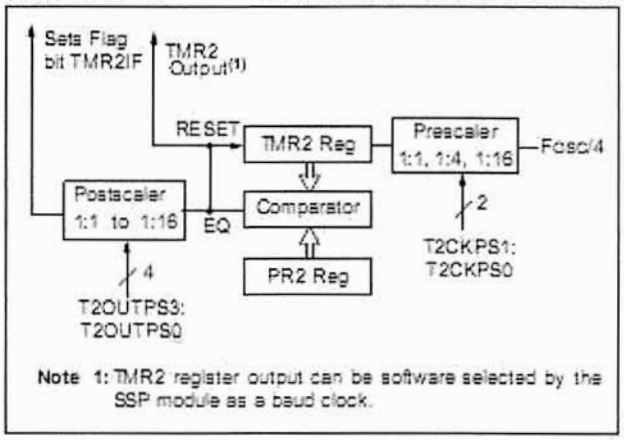
The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

Timer2 can be shut-off by clearing control bit TMR2ON (T2CON<2>), to minimize power consumption.

Register 7-1 shows the Timer2 control register.

Additional information on timer modules is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



Note 1: TMR2 register output can be software selected by the SSP module as a baud clock.

REGISTER 7-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
0010 = 1:3 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2 **TMR2ON**: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

8.0 CAPTURE/COMPARE/PWM MODULES

Each Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM Master/Slave Duty Cycle register

Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger. Table 8-1 and Table 8-2 show the resources and interactions of the CCP module(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 Module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer1.

CCP2 Module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Additional information on CCP modules is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023) and in application note AN594, "Using the CCP Modules" (DS00594).

TABLE 8-1: CCP MODE - TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 8-1: CCP1CON REGISTER/CCP2CON REGISTER (ADDRESS: 17h/1Dh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CCPxX:CCPxY**: PWM Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0 **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)
11xx = PWM mode

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Tournez la page S.V.P.

8.3 PWM Mode (PWM)

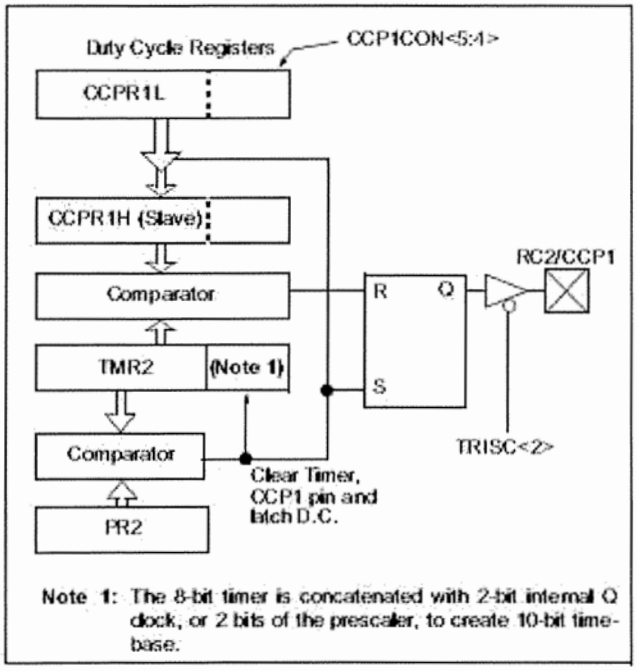
In Pulse Width Modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 8-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 8.3.3.

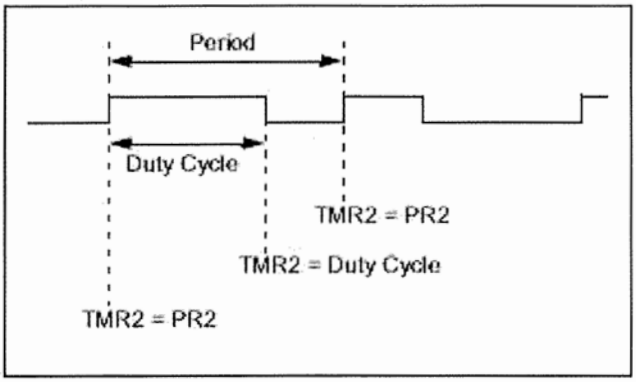
FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The 8-bit timer is concatenated with 2-bit internal Q clock, or 2 bits of the prescaler, to create 10-bit time-base.

A PWM output (Figure 8-4) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 8-4: PWM OUTPUT



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(\text{PR2}) + 1] \cdot 4 \cdot \text{Tosc} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 7.1) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM duty cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot \text{Tosc} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitch-free PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock, or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

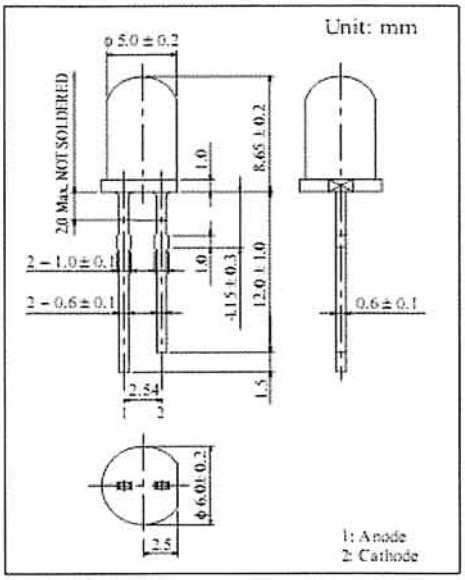
The maximum PWM resolution (bits) for a given PWM frequency is given by the formula:

$$\text{Resolution} = \frac{\log\left(\frac{\text{Fosc}}{\text{Fpwm}}\right)}{\log(2)} \text{ bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

Round Type

ϕ 5.0 mm Series



Conventional Part No.	Global Part No.	Lighting Color
LN81RPHL	LNG801RDD	Orange
LN81RCPHL	LNG801LDD	Orange
LN81WPHL	LNG801WDD	Orange
LN81CPHL	LNG801CDD	Orange

■ Absolute Maximum Ratings (T_a = 25°C)

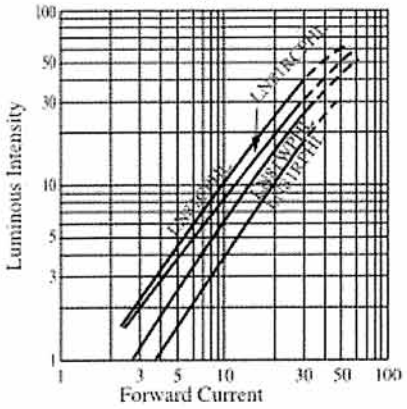
Lighting Color	P_D(mW)	I_F(mA)	I_{FP}(mA)*	V_R(V)	T_{opr}(°C)	T_{stg}(°C)
Orange	90	30	150	3	−25 ~ +80	−30 ~ +100

Pulse width 1 msec. The condition of I_{FP} is duty 10%, Pulse width 1 msec

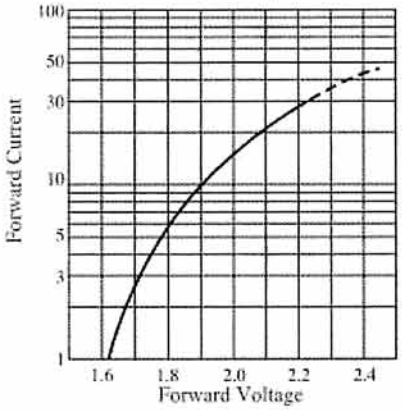
■ Electro-Optical Characteristics (T_a = 25°C)

Conventional Part No.	Lighting Color	Lens Color	I_O		I_F	V_F		λ_P	$\Delta\lambda$	I_F	I_R	
			Typ	Min		Typ	Max	Typ	Typ		Max	V_R
LN81RPHL	Orange	Red Diffused	10.0	5.0	20	2.1	2.8	630	40	20	10	3
LN81RCPHL	Orange	Red Clear	20.0	8.0	20	2.1	2.8	630	40	20	10	3
LN81WPHL	Orange	White Diffused	15.0	6.0	20	2.1	2.8	630	40	20	10	3
LN81CPHL	Orange	Clear	25.0	10.0	20	2.1	2.8	630	40	20	10	3
Unit	—	—	mcd	mcd	mA	V	V	nm	nm	mA	μA	V

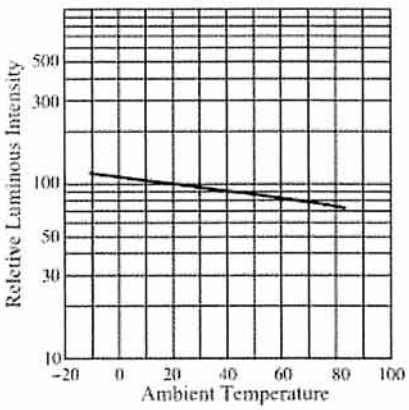
I_O — I_F



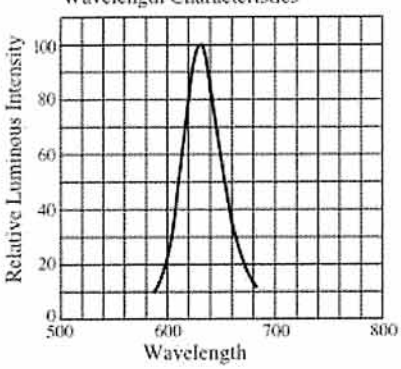
I_F — V_F



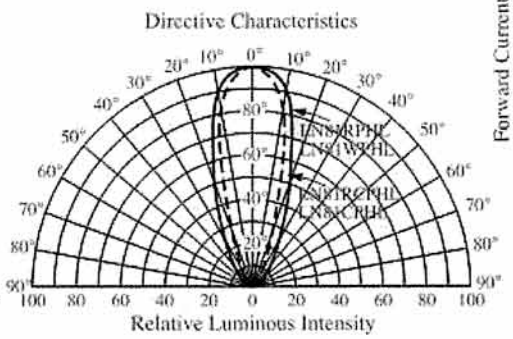
I_O — T_a



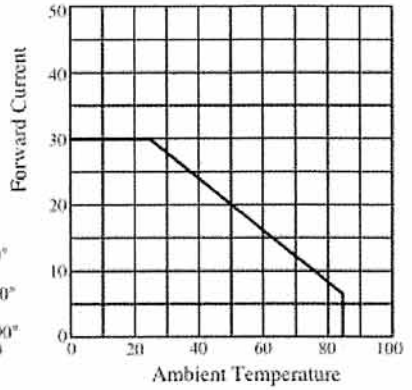
Relative Luminous Intensity Wavelength Characteristics



Directive Characteristics



I_F — T_a



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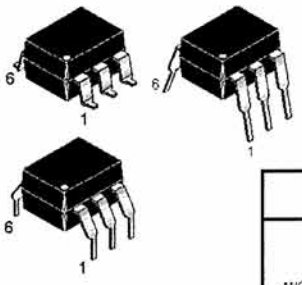
FAIRCHILD
SEMICONDUCTOR™

6-PIN PHOTOTRANSISTOR OPTOCOUPLERS

CNX35U CNX36U CNX38U CNX39U

DESCRIPTION

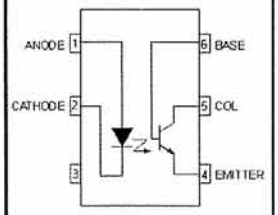
The CNX35U, CNX36U CNX38U and CNX39U are optically coupled isolators consisting of an infrared emitting GaAs diode and a silicon NPN phototransistor with accessible base. These devices are housed in 6-pin dual-in-line packages (DIP).



FEATURES

- High output/input DC current transfer ratio
- Low saturation voltage
- UL recognized (File # E90700)
- VDE recognized (File # 94766)
  -Ordering option '300' (e.g. CNX35U.300)

SCHEMATIC



APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs
- Appliance sensor systems
- Industrial controls

Parameters	Symbol	Device	Value	Units
TOTAL DEVICE Storage Temperature	T_{STG}	All	-55 to +150	°C
Operating Temperature	T_{OPR}	All	-40 to +100	°C
Lead Solder Temperature	T_{SOL}	All	260 for 10 sec	°C
EMITTER Continuous Reverse Voltage	V_R	All	5	V
Continuous Forward Current	I_F	All	100	mA
Forward Current - Peak (10 µs pulse, δ = 0.01)	I_F(pk)	All	3.0	A
Total Power Dissipation up to 25°C Ambient	P_D	All	200	mW
Derate Linearly from 25°C		All	2.0	mW/°C
DETECTOR Collector to Emitter Voltage (open base)	V_{CEO}	CNX38U	80	V
		CNX35U, CNX36U, CNX39U	30	
Collector to Base Voltage (open emitter)	V_{CBO}	CNX38U	120	V
		CNX35U, CNX36U, CNX39U	70	
Emitter to Collector Voltage (open base)	V_{ECO}	All	7	V
DC Collector Current	I_C	All	100	mA
Detector Power Dissipation up to 25°C Ambient	P_D	All	200	mW
Derate Linearly from 25°C		All	2.0	mW/°C

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FAIRCHILD
SEMICONDUCTOR™

6-PIN PHOTOTRANSISTOR OPTOCOUPLERS

CNX35U CNX36U CNX38U CNX39U

TRANSFER CHARACTERISTICS (T_A = 25°C Unless otherwise specified.)

DC Characteristics	Test Conditions	Symbol	Device	Min	Typ	Max	Units
Output/Input Current Transfer Ratio	I_F = 10 mA, V_{CE} = 0.4 V	CTR	CNX35U	40		160	%
			CNX39U	60		100	
			CNX36U	80		200	
	I_F = 10 mA, V_{CE} = 10 V		CNX38U	70		210	
	I_F = 16 mA, V_{CE} = 0.4 V			50			
	I_F = 2 mA, V_{CE} = 5 V		All	15			
Collector-Emitter Saturation Voltage	I_F = 10 mA, I_C = 2 mA	$V_{CE(SAT)}$	CNX35U, CNX39U		0.15	0.4	V
	I_F = 10 mA, I_C = 4 mA		CNX36U		0.19	0.4	
	I_F = 16 mA, I_C = 2 mA		CNX38U		0.2	0.4	
AC Characteristics	**Test Conditions**	**Symbol**	**Device**	**Min**	**Typ**	**Max**	**Units**
Non-Saturated Switching Times Turn-On Time See Fig. 1 and Fig. 2	R_L = 100 Ω, I_C = 2 mA, V_{CC} = 5 V	t_{on}	CNX35U			20	µs
			CNX39U			20	
			CNX36U			20	
	R_L = 100 Ω, I_C = 4 mA, V_{CC} = 5 V		CNX38U			20	
Turn-Off Time See Fig. 1 and Fig. 2	R_L = 100 Ω, I_C = 2 mA, V_{CC} = 5 V	t_{off}	CNX35U			20	µs
			CNX39U			20	
			CNX36U			20	
	R_L = 100 Ω, I_C = 4 mA, V_{CC} = 5 V		CNX38U			20	
Saturated Switching Times Turn-On Time See Fig. 1 and Fig. 2	R_L = 1 kΩ, I_C = 2 mA, V_{CC} = 5 V	t_{on}	CNX35U			50	µs
			CNX39U			50	
			CNX36U			50	
	R_L = 1 kΩ, I_C = 4 mA, V_{CC} = 5 V		CNX38U			50	
Turn-Off Time See Fig. 1 and Fig. 2	R_L = 1 kΩ, I_C = 2 mA, V_{CC} = 5 V	t_{off}	CNX35U			50	µs
			CNX39U			50	
			CNX36U			50	
	R_L = 1 kΩ, I_C = 4 mA, V_{CC} = 5 V		CNX38U			50	

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6-PIN PHOTOTRANSISTOR OPTOCOUPLERS

CNX35U CNX36U CNX38U CNX39U

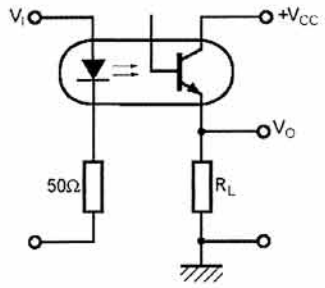


Fig. 1 Switching Test Circuit

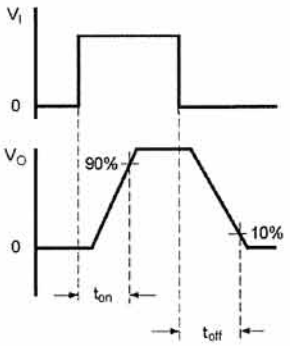


Fig. 2 Switching Test Waveforms

Fig. 3 LED Forward Voltage vs. Forward Current

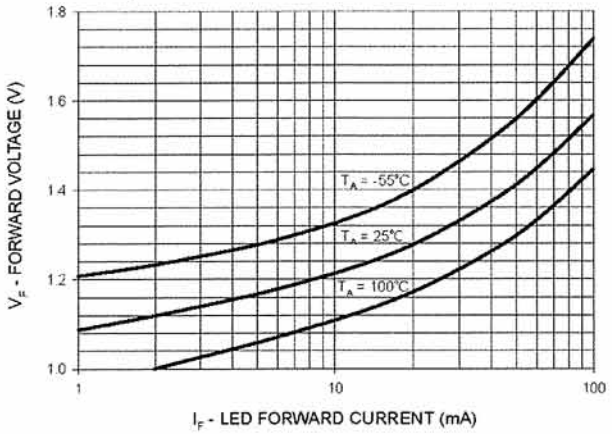


Fig. 4 Normalized CTR vs. Forward Current

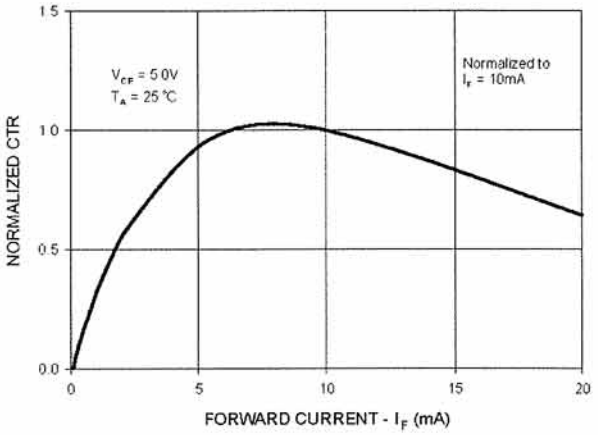


Fig. 5 Normalized CTR vs. Temperature

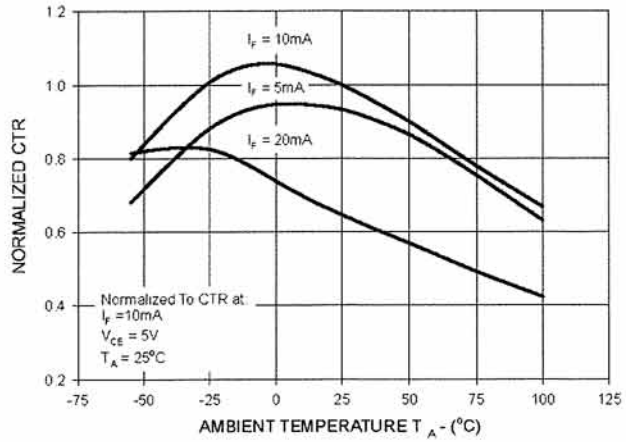
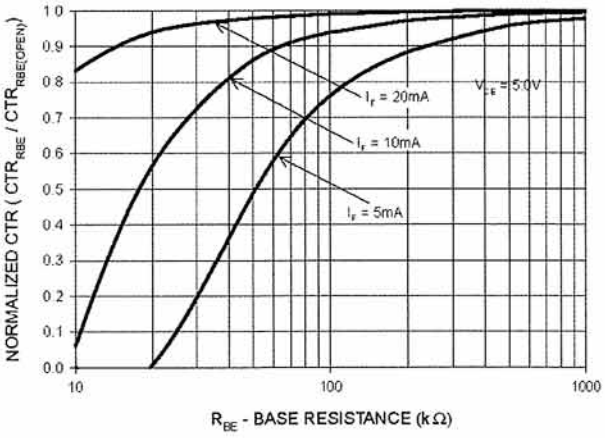


Fig. 6 CTR vs. RBE (Unsaturated)



Document Ressource 4 : résistances

Série de résistances:
Toutes les valeurs de résistance n'existent pas. Voici suivant la série les valeurs possibles sur une décade: pour trouver la suite de la série, il suffit de multiplier par 10!

Série E3																
	100							220					470			
Série E6																
	100			150			220			330			470			680
Série E12																
	100	120		150	180		220	270		330	390		470	560		680	820
Série E24																
	100	110		120	130		150	160		180	200		220	240		270	300
	330	360		390	430		470	510		560	620		680	750		820	910
Série E48																
	100	105	110	115	121	127	133	140	147	154	162	169	178	187	196	205
	215	226	237	249	261	274	287	301	316	332	348	365	383	402	422	442
	464	487	511	536	562	590	619	649	681	715	750	787	825	866	909	953
Série E96																
	100	102	105	107	110	113	115	118	121	124	127	130	133	137	140	143
	147	150	154	158	162	165	169	174	178	182	187	191	196	200	205	210
	215	221	226	232	237	243	249	255	261	267	274	280	287	294	301	309
	316	324	332	340	348	357	365	374	383	392	402	412	422	432	442	453
	464	475	487	499	511	523	536	549	562	576	590	604	619	634	649	665
	681	698	715	732	750	768	787	806	825	845	866	887	909	931	953	976

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March 1998

FAIRCHILD SEMICONDUCTOR™

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

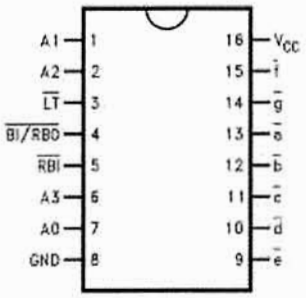
The 'LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 µA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

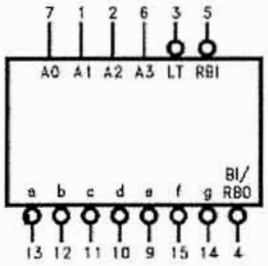
Connection Diagram

Dual-In-Line Package

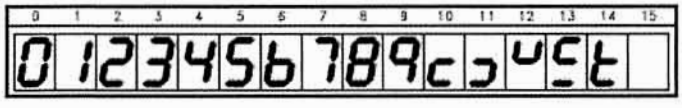


Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$ – $\overline{g}$	*Segment Outputs (Active LOW)

Logic Symbol



Numerical Designations—Resultant Displays



DOCUMENTS RÉPONSE

Document Réponse 1 : codage des registres
Document Réponse 2 : tableau de fonctionnement du pont en H
Document Réponse 3 : incrémentation de la fréquence cardiaque
Document Réponse 4 : influences sur le comportement du pont
Document Réponse 5 : tableau indicateurs environnementaux
Document Réponse 6 : affichage de la fréquence cardiaque

Modèle ENSD ©NEOPTEC

Nom :
(Suivi, s'il y a lieu, du nom d'épouse)

Prénom :

N° d'inscription :

Né(e) le : / /

(Le numéro est celui qui figure sur la convocation ou la feuille d'émargement)

Concours	**Section/Option**	**Epreuve**	**Matière**

Documents réponse 1 à 6

Document Réponse 1 : codage des registres

Registre	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON										
PR2										
Registre de comparaison										
CCPR1L										
CCP1CON										

Document Réponse 2 : tableau de fonctionnement du pont en H

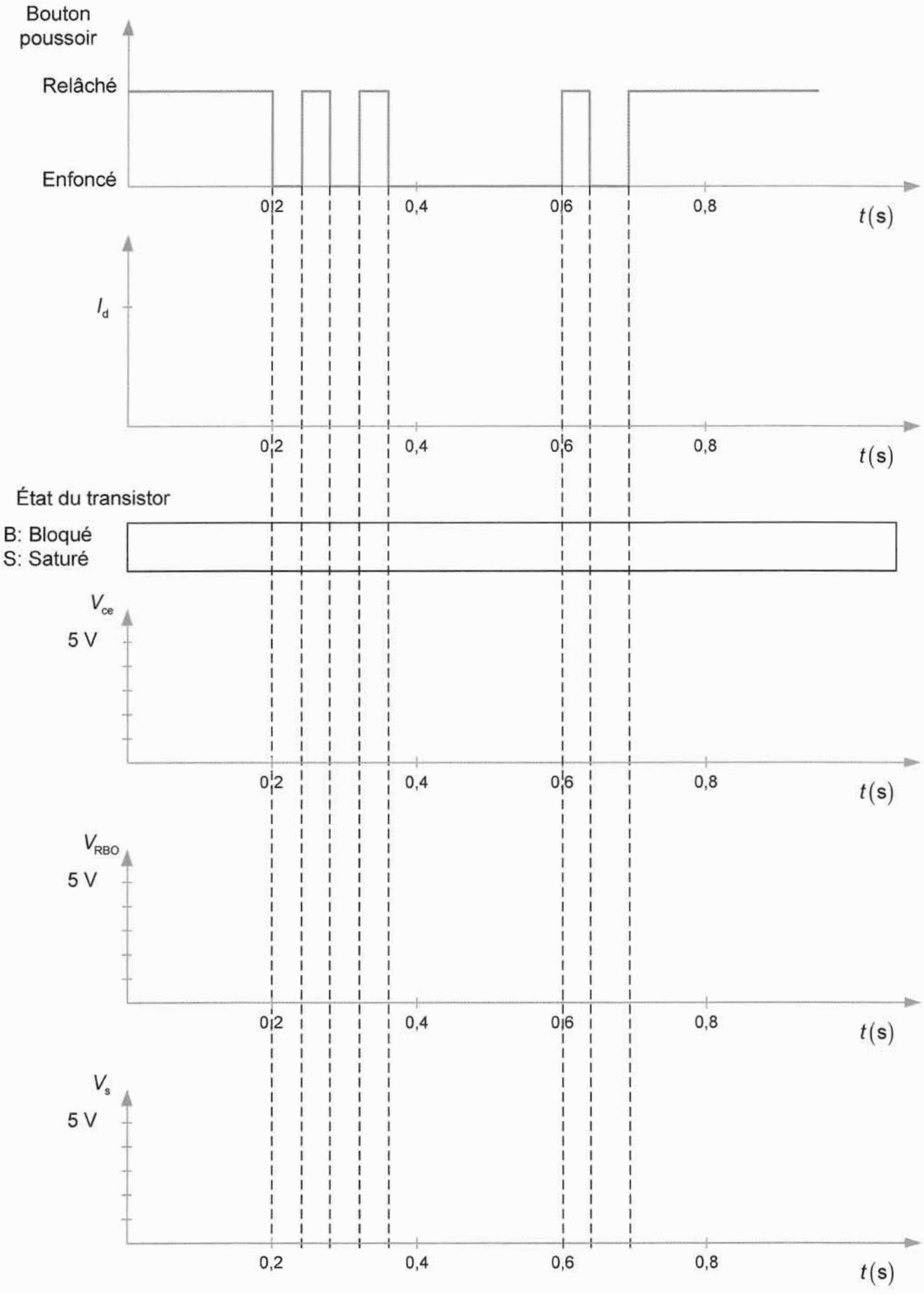
*Input*1	*Input*2	A	T05	T06	Mos T01	Mos T02	Mos T03	Mos T04	Moteur

Notation imposée :

P = Passant

B = Bloqué

Document Réponse 3 : incrémentation de la fréquence cardiaque



Modèle ENSD ©NEOPTEC

Nom :
(Suivi, s'il y a lieu, du nom d'épouse)

Prénom :

N° d'inscription :

Né(e) le : / /

(Le numéro est celui qui figure sur la convocation ou la feuille d'émargement)

Concours	Section/Option	Epreuve	Matière

Documents réponse 1 à 6
suite et fin

Document Réponse 4 : influences sur le comportement du pont

	Grandeurs influentes		
	E_{pont} ↗	épaisseur ↗	largeur ↗
Influence sur la déformation	↗ ↘ → ?	↗ ↘ → ?	↗ ↘ → ?
Influence sur la résistance	↗ ↘ → ?	↗ ↘ → ?	↗ ↘ → ?

Légende des symboles

- ↗ Induit une augmentation de la grandeur caractéristique
- ↘ Induit une diminution de la grandeur caractéristique
- → N'a pas d'influence sur la grandeur caractéristique
- ? Il n'y a pas assez d'éléments pour se prononcer

- Le critère retenu pour juger de la déformation est la valeur maximale du déplacement des points de la ligne moyenne

- Le critère retenu pour juger de la résistance est la valeur maximale de la contrainte normale dans la poutre

Document Réponse 5 : tableau indicateurs environnementaux

	Masse Volumique ρ	Module de Young E	Phase de fabrication	Recyclage	indice de performance
			GWP	GWP	
	(Kg/m^3)	(GPa)	(Kg eq CO_2/Kg)	(Kg eq CO_2/Kg)	
Acier courant	7850	207,5	2,5	0,69	
Acier inoxydable	7850	202	5,15	1,43	
Thermoplastique (PVC)	1440	3,1	2,4	1	
Thermoplastique (ABS)	1110	2	3,45	1,45	
Aluminium	2700	70	12,05	1,09	
Fonte grise	7138	109	1,02	0,305	

(données issues du logiciel CES edupack 2009)

Document Réponse 6 : affichage de la fréquence cardiaque